TSV reveal process developments for 2.5D integration

Chongshen Song[1, 2, *], Lei Wang[1, 2], Zhun Wang[1], Daquan Yu[1, 2], Wenqi Zhang[1]
[1] National Center for Advanced Packaging (NCAP China), Wuxi 214135, China
[2] Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
*Email: chongshensong@ncap-cn.com, Tel.: +86-510-6667 9337

Abstract

2.5D integration using TSV silicon interposer has attracted much attention in recent years for both front-end foundries and back-end packaging houses. TSV back revealing is one of the key process modules for the fabrication of 2.5D interposer. Two kinds of process flows for TSV revealing are introduced and compared in this paper. The first one uses Si-Cu co-polishing for copper revealing, which can compensate the total thickness variation (TTV) of TSV tips, but the passivation opening on the back side of the TSVs becomes more and more difficult when the TSV size is scaling down. The second one reopens the backside of the TSVs after backside polymer passivation by mask-free plasma etching, which is advantageous for small TSVs but needs to control the TTV strictly. Fabrication results using these two process flows are given and discussed.

Introduction

Through-Silicon Vias (TSVs) offer a method for improving electrical signal speeds by reducing interconnect length. Although TSVs can be fabricated directly on active silicon dies, the design, EDA tools and process yield are far from ready, so it is very difficult for high volume use at present. 2.5D integration using TSV interposer, where TSVs are fabricated in passive silicon wafers, has attracted much attention in recent years for both front-end foundries and back-end packaging houses. The first few applications of TSVs are also in Field Programmable Gate Arrays (FPGAs) [1], where 2.5D TSV integration is used.

The fabrication of 2.5D TSV interposer mainly uses via first scheme, which means that the TSVs are firstly fabricated from the front side of the silicon wafer before any other process steps, as shown in fig.1. After TSV formation and front side RDL & bumping fabrication, the wafer will be bonded with a carrier wafer, followed by wafer back thinning and TSV reveal. Then backside RDL and bump will be formed. Finally the interposer wafer will be de-bonded from the carrier wafer and diced for 2.5D system assembly.

Upon afore-mentioned information, the fabrication of a TSV interposer can be divided into four process modules, which are TSV formation, RDL and bumping, TSV revealing, bonding/de-bonding, respectively. TSV formation includes several special process steps optimized for high aspect ratio structures, such as TSV etching, liner deposition, conductive filling, planarization, etc, which have been studied for many years and have several near-mature solutions. RDL and bumping can be realized through foundry based or packaging house based processes, which is mature technology. The other two process modules are still with challenges and need several improving work.

This paper will focus on TSV revealing process developments for 2.5D integration. As the supply chain for

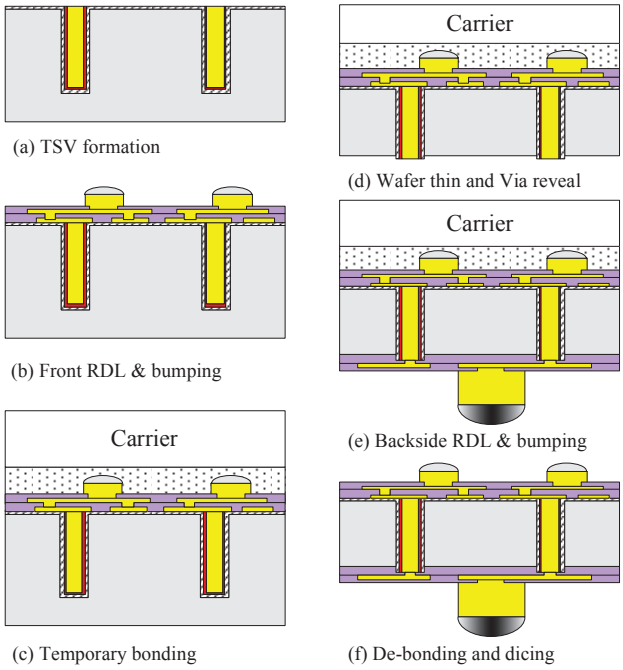

Fig. 1 Typical Process flow of TSV interposer.

TSV technology is not clear yet, TSV reveal may be realized in a place different from the place where the TSV is fabricated, so the TSV revealing is a relatively independent process. A general process flow for TSV reveal has been proposed by several industry players [2-4]. Backside grind and silicon CMP (optional) is firstly conducted after carrier wafer bonding and stops at a distance of about 10~20μm to the back end of the TSVs, which remains encased within the thinned silicon wafer to ensure that no copper becomes exposed. Then dry etching is done to recess the silicon. The height of the exposed TSV pillars is in the range of 2μm to 6μm, depending on the dielectric of subsequent Re-Distribution Layer (RDL) and bump process, and the desired TTV of the TSV pillars is below 1-2μm across the wafer. The best dielectric choice may vary depending on the specific application requirements, such as planarity requirements or high frequency operation. Inorganic, low temperature chemical vapor deposition (CVD) oxide and nitride are preferred to organic dielectrics. Subsequently, dielectric CMP is conducted to expose Cu with smooth dielectric insulation between TSVs and following RDL/bump processing [2].

Such a general process flow uses dry etching, dielectric CVD and CMP for via reveal, which need expensive equipment, so the cost is very high. Furthermore, as dielectric CMP is used to expose the copper, the total thickness variation (TTV) of the TSV pillars after dry etching need to be strictly controlled. As mentioned above, the TTV may need to be

978-1-4799-2834-7/13/$31.00 ©2013 IEEE

controlled below 1-2μm, which is very difficult considering that the incoming wafers to via reveal can have significant compounded variation, such as TSV depth uniformity, carrier wafer thickness uniformity, bonding glue thickness uniformity and silicon thickness uniformity after wafer grinding [4]. So the process yield is challenging. To improve the process yield and decrease the process cost, new process flows need to be developed.

Considering the requirements for low cost and process controllability for 2.5D integration, two process flows are proposed and evaluated in this paper. Experiment results will be given and discussed.

Experiments

TSVs with a diameter of 30μm and a depth of about 160μm are firstly fabricated in 200mm silicon wafer, the cross section view of the TSVs after copper plating filling is shown in Fig.2. After front RDL and micro bump are formed, the silicon wafer is edge trimmed and bonded with glass carrier wafer by temporary bonding glue, then the bonded wafer pairs are ready for TSV revealing experiments.

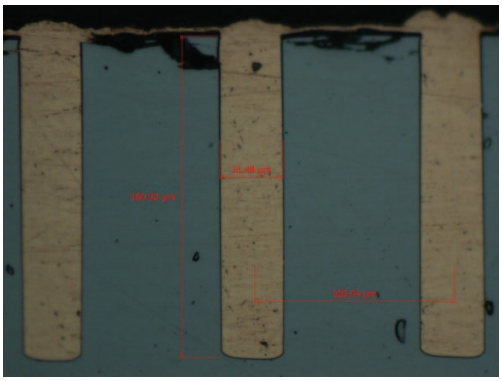

Fig.2 Cross section view of the TSVs filled with copper.

Considering the requirements of low-cost and robust process controllability for 2.5D interposers, two process flows are proposed, as shown in Fig.3.

The first flow starts with back grinding and Si-Cu co-polishing to reveal the filling copper directly, as shown in Fig.3 (1a), then polymer passivation layer is formed and patterned to re-expose the TSV copper, as shown in Fig.3 (1b), finally backside RDL is fabricated to interconnect the TSV out from the backside of the interposer wafer, as shown in Fig.3 (1c). As the 2.5D interposer is normally fabricated in passive silicon, possible copper contamination from Si-Cu co-polishing may not be a big concern. Furthermore, as the silicon surface and TSV copper on the wafer backside is at the same level after Si-Cu co-polishing, any thickness variation can be compensated, which is key for robust process controllability, especially when the in-coming wafers have many variations.

As of the second process flow, grinding and silicon dry etching is firstly conducted to expose the TSV pillars keeping the TSV copper sealed with oxide liner, as shown in Fig.3 (2a). Then low temperature oxide and polymer layer is formed on backside of the interposer wafer, as shown in Fig.3 (2b). As the existence of surface height difference near the TSV pillars, and the polymer is formed by spin-coating method, the polymer upon TSV pillars are much thinner than that at other area of the wafer backside. After mask-free polymer etching, the polymer upon TSV pillars is firstly cleaned and the oxide liner on TSV pillars is revealed. The oxide layer is etched afterwards, and the TSV copper is revealed while keeping the back surface of the interposer wafer covered with insulation layer, as shown in Fig.3 (2c). Finally, backside RDL is fabricated to connect the TSVs, as shown in Fig.3 (2d). This flow is based on aforementioned general method but does not use CMP treatment for final TSV copper reveal. Although overall cost can be reduced, the TTV of the TSV pillars after silicon dry etching still needs to be controlled strictly.

Optical microscope and cross section inspection is used to evaluate the process quality. Experimental results after specific process steps will be given in next part, and the Pros and Cons of these two process flows for TSV revealing will also be discussed.

Results and discussions

Using the first flow, wafer grinding and Si-Cu co-polishing are conducted on TSV wafers to reveal the TSV copper directly by using DGP 8761 machine from Disco. Fig. 4 shows the fabrication results after the TSV copper is revealed by CMP treatment, which don't have selectivity

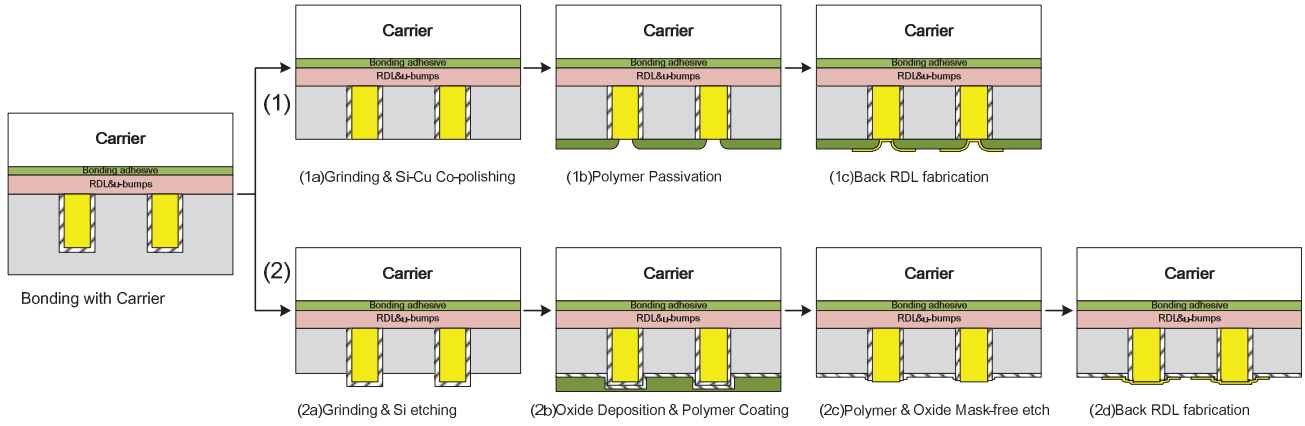

Fig.3 Proposed process flows for TSV Revealing

between silicon and copper. From Fig.4, it can be seen that the back opening size of the TSVs is about 27μm, which is a little smaller than that at front opening.

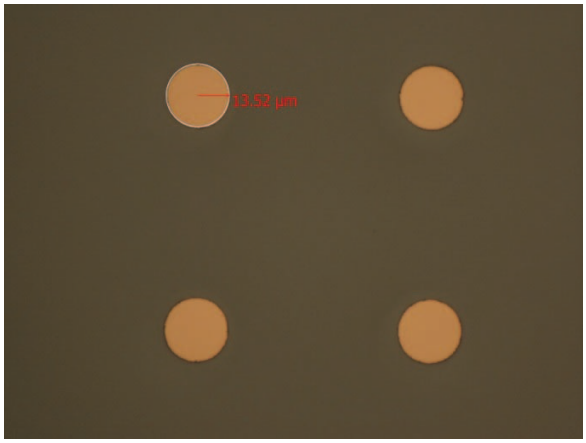

Fig.4 Optical Microscope view after copper reveal by Si-Cu co-polishing under the first process flow.

After the copper is revealed, a polymer layer is spin-coated and patterned on back side of the TSVs, followed by low temperature (below 200 °C) curing treatment. The passivation layer has a thickness of about 6μm after curing, the opening size at the bottom of TSV is designed to be 15μm in diameter but after polymer development and curing, the actual opening diameter is about 16μm, as shown in Fig.5. It can be seen from Fig.5 that the passivation opening has misalignment with TSV back, when the TSV size is scaling down, this problem will become worse.

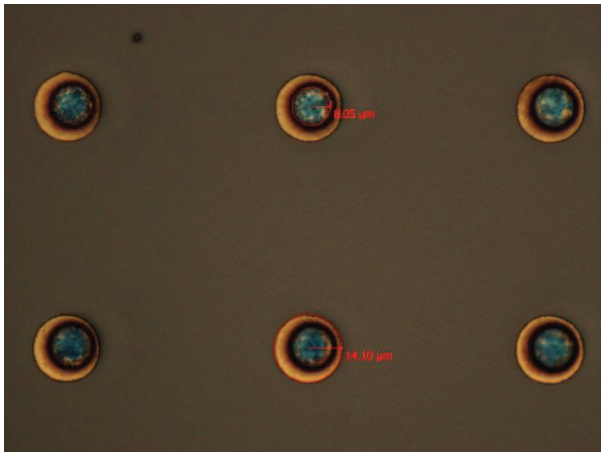

Fig.5 Optical Microscope view after backside passivation pattern opening under the first process flow.

Then backside RDL is formed using semi-additive plating process to interconnect the TSV out. Fig.6 shows the optical microscope view after RDL fabrication. As the existence of a via hole between TSV and corresponding RDL, there is a cave structure on backside of the TSV, as shown in Fig.6. The cross section view of the interposer chip after backside process is shown in Fig.7. Although the TSV is electrically interconnected with RDL, the misalignment is very high, which leads to electrical short between backside RDL and silicon substrate. When the TSV size is scaling down, this problem will become worse and lithography alignment and process improvements are needed.

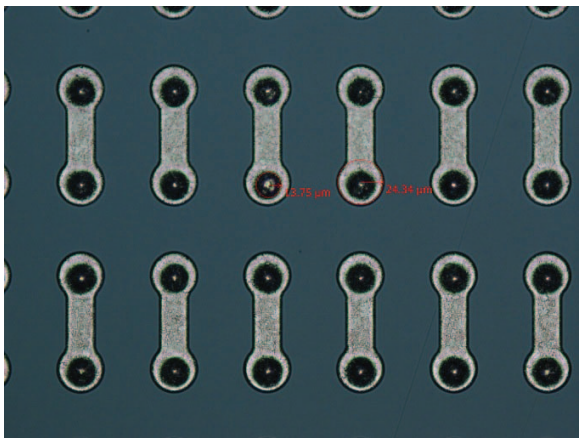

Fig.6 Surface microscope view after backside RDL fabrication under the first process flow.

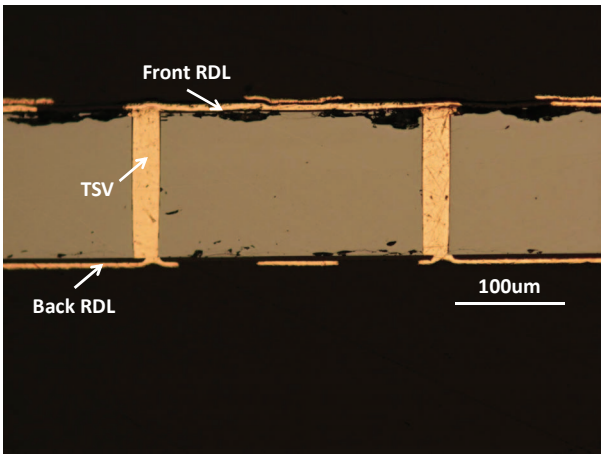

Fig.7 Cross section view after backside RDL fabrication under the first process flow.

Using the second process flow, experiments have also been conducted. After wafer grinding and silicon dry etching, TSV pillars are formed. Here the TSV copper is still sealed with liner oxide layers. Then another oxide layer with a thickness of 1um is deposited on the backside of the wafer for backside passivation. Then the wafer is coated with a polymer layer using spin-coating process. As the polymer layer on top of the TSV pillars is much thinner than that on the other area of the wafer backside, mask-free polymer and oxide etching is used to reveal the TSV copper keeping the silicon backside passivated. Fig. 8 shows the surface view after TSV copper is revealed. As the existence of thickness variation of TSV depth, carrier wafer, bonding glue and the non-uniformity of grinding and dry etching, the height of the TSV pillar after copper reveal may have large TTV across the wafer. According to the initial results, the TTV may be as large as 15um, which needs to be improved. After copper reveal, backside RDL is fabricated using semi-additive plating

process to interconnect the TSV out, the cross section view of which is shown in Fig. 9.

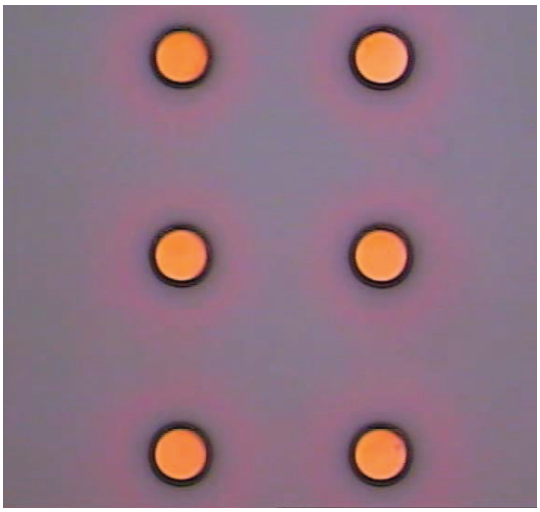

Fig.8 Surface microscope view after copper review under the second process flow.

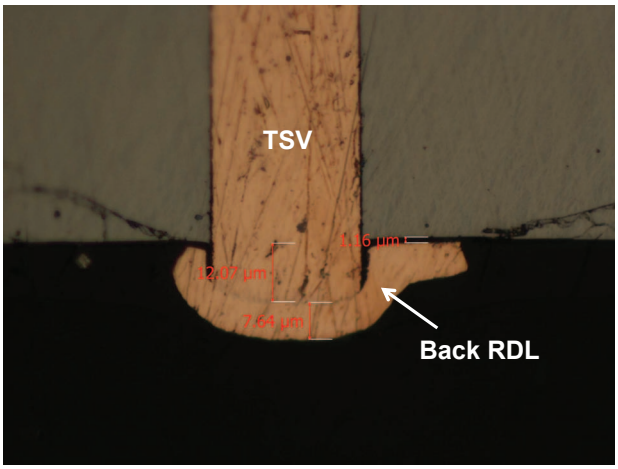

Fig.9 Cross section view after back RDL fabrication under the second process flow.

From Fig.9, it can be seen that the TSV pillar is as high as 12µm above the back surface of the interposer wafer, and the backside RDL needs to cover such a high step for enough interconnection performance. This step should be reduced in future to ensure the interconnection performance, so TTV control including TSV depth, carrier thickness, bonding glue, grinding, etc. needs to be improved. As the back RDL is directly interconnected with back tip of the TSVs under the second process flow, so there will not be much different when the TSV size is scaling down.

Summarizing the discussions, we can make a comparison between the two TSV revealing process flows proposed in this paper and the conventional method. The Pros and Cons are listed in Table I. Although the proposed process flows can be used for TSV reveal, there are still some constrains, which need to be improved in future work.

Table I Comparison of different revealing flows

Revealing flow	Pros.	Cons.
Conventional method [2]	suitable for every situation; Good scaling performance;	Need CMP treatment, so cost is high; TTV control difficult;
Proposed flow 1	Can compensate TTV of other steps; Process simple; Low cost;	Potential Cu contamination, Not suitable for active silicon; Some scaling constrains;
Proposed flow 2	suitable to every situation; Good scaling performance; Don't need CMP, lower cost;	TTV control difficult;

Conclusions

Two process flows for TSV revealing have been proposed and discussed in this paper. The Si-Cu co-polishing method is simple with low cost, and can compensate the TTV from other process steps, but this method has potential copper contamination problem and may become challenging when the TSV size is scaling down. The second process flow doesn't use CMP and back RDL is directly interconnected with back tips of the TSVs, so it has good TSV scaling performance. But the TTV should be controlled strictly, which need to be improved in future work.

Acknowledgments

The authors acknowledge the support from the National Science and Technology Major Project under contract No. 2009ZX02038 and No. 2013ZX02501.

References

1. Xilinx October 2011 white paper announced shipment of world's first interposer based highest capacity FPGA in September 2011.
2. Niranjan Kumar, et al, "Robust TSV via-middle and Via-Reveal Process Integration Accomplished through Characterization and Management of Sources of Variation", Proc. 62nd Electronic Components and Technology Conf, San Diego, CA, May 29 ~ Jun 1, 2012, pp. 787-793.
3. Kath Crook, et al, "Dielectric Stack Engineering for Via-Reveal Passivation", Proc. 63rd Electronic Components and Technology Conf, Las Vegas, May 28-31, 2013, pp. 576-580.
4. B.-K. Huang, et al, "Integration Challenge of TSV backside Via Reveal Process", Proc. 63rd Electronic Components and Technology Conf, Las Vegas, May 28-31, 2013, pp. 915-917.