Investigation of temporary bonding and release processes for TSV with copper pillar bumps

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***Abstract*—Temporary bonding and release processes are regarded as the critical technologies in 2.5D and 3D IC integration. The process is especially challenging when the device contains high topography structures like copper pillar bumps. This paper presents the results of simulation, bumping process, wafer temporary bonding, thinning and debonding. Through careful consideration and optimization of the above mentioned aspects, TSV wafers with 30 µm copper pillar bumps can be successfully released using the thermal-sliding debonding mechanism.**

Keywords—temporary bonding; copper pillar bump; style; 3D integration; TSV; debonding

I. INTRODUCTION

Through silicon vias (TSVs) are regarded as a key enabling technology for 3D IC integration which assists in the realization of highly miniaturized and complex next-generation systems. With the efforts of semiconductor manufacturers, the latest commercial product to utilize TSV technology is the Xilinx Vitrex-7 which uses a 2.5D interposer fabricated by TSMC with Amkor µ-bump assembly and an Ibiden organic substrate. According to the cost modeling calculations of Yole Développement, the bonding/debonding and the thinning/TSV reveal processes take up 20% and 19% of the total manufacturing cost, respectively, for a typical 100 µm thick silicon interposer with TSVs and 3 Cu damascene layers[1-3]. The higher cost in these processes is attributable to the materials and equipment costs, yield, throughput, and the actual processing. Temporary wafer bonding, thinning and debonding processes are some of the critical technologies identified as needing rapid improvement.

In Fig.1 is shown a typical temporary bonding structure for 2.5D TSV interposer. The first critical aspect of this part of the processes is the interfacial bonding material (or called bonding adhesives). It must combine a variety of properties and functions that are physically, chemically and thermally stable during the thinning and subsequent backside processing steps. In addition, the material should be easily debonded after wafer thinning and the backside processes. The ability of the bonding material to be very uniform in thickness across the wafer enables a very low total thickness variation (TTV) after thinning, TSV reveal process, backside RDL and bumping. This becomes extremely important when the device wafer contains tall topographic structures, such as Cu pillars or micro-bumps, which may range from 10 to 100 µm. The challenge here is to find a temporary bonding material that is able to maintain a low TTV level for different topographic structures. Backside grinding of ultra-thin wafers requires very low TTV as well as a void-free temporary bonding layer.

The second critical aspect is the choice of wafer handlers. Glass and silicon have been used for this purpose for many years. Each has its advantages and limitations. Of concerns here are mechanical, thermal, and electrical properties of the semiconductor wafers during TSV wafer manufacturing. Glass is transparent, making it easy for bonding alignment and voids detection. But glass and silicon have a mismatch in coefficient of thermal expansion (CTE), which can result in warpage problem. The temporary handler/wafer stack needs to handle the warpage issue throughout the process, which may include temperature excursions. This is because, among other reasons, the standard chuck is only able to tolerate a certain degree of warpage [4]. The use of glass or silicon handler may have different implications on the chucking technology because of compatibility issue. For example, a vacuum chuck may work for both glass and silicon, but an electrostatic chuck may require a metal layer on the glass handler.

The third critical aspect is separation the product wafer from its handler wafer. A wide variety of approaches have been proposed and are being developed today. These include thermal-sliding [5], chemical-assisted release [6], laser-assisted release [7], and room-temperature mechanical peeling release [8]. The selection a specific debonding technology depends on temperature limitations and throughput requirements, in addition to being consistent with the requirements of the overall process flow, for example low-melting point solders or high-topography structures. Therefore, ease of debonding becomes a critical part of the overall process.

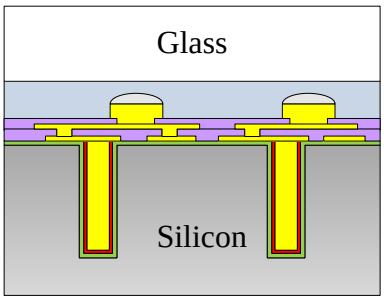

Fig.1 Typical temporary bonding structure for TSV interposers with RDL and micro-bumps

In this paper, we report our recent progress on the temporary bonding and release processes for thinning TSV wafers with copper pillar bumps.

II. FINITE ELEMENT ANALYSIS

The commercial finite element analysis (FEA) software ANSYS is used in this study. A 2D model is built to simulate the debonding effect on copper pillar bumps. In the simulation, the silicon device wafer is 775 μm in thickness and 3mm in width, same size with the glass carrier. The copper pillars are 30 μm in diameter and 60 μm in pitch, and 13.5 μm in height. The bonding adhesives thickness is varied from 20 μm to 100 μm. The bottom of silicon wafer is fixed. In Fig.2 is shown an overall stress distribution and local stress distribution in the outer bumps area during slide debonding.

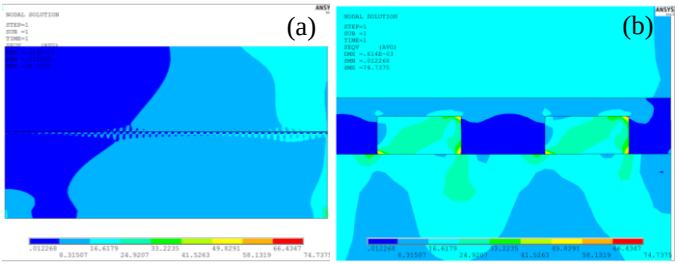

Fig.2 Overall stress distribution (a) and local stress distribution (b) for temporary bonded pairs

When thermal-release bonding adhesives are heated, their viscosity greatly diminishes, making it deform easily under an applied sliding force. From Fig.2(b), the corners of copper pillar bumps suffer from high stress level, especially at the outer zone of the wafer. This portion of copper pillars may be damaged and dropped by the shear force from the bonding adhesives. When the thickness of the bonding adhesives increases from 15 μm to 100 μm, the maximum stress increases. To control the TTV for high topography surfaces, thicker bonding adhesives are required with the consequence that the thicker bonding layer will lead to higher stress during debonding. Therefore, the thickness of the coating adhesives should be carefully optimized to achieve a sufficiently robust bonding during thinning and other backside processes, but with less shear forces during debonding.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. TSV and Cu pillar fabrication

Eight-inch, (100) silicon wafers 775 μm thick are etched by deep reactive ion reactive etching (DRIE) tool to form 30 μm in diameter cylindrical vias to a depth of 160 μm. After the step s of photoresist stripping and via residue cleaning, a layer of silicon dioxide (SiO_2) is deposited by Tetraethyl orthosilicate (TEOS) plasma enhanced chemical vapor deposition (PECVD). Next, a composite barrier and seed layer of Ti/Cu is deposited by physical vapor deposition (PVD). The via conductor is copper, which is filled by bottom-up electroplating. After over burden removal by chemical mechanical planarization (CMP) process, redistribution layers (RDL) are formed by the application of repeated photolithography, sputtering and electroplating steps. The under bump metallurgy (UBM) is then PVD deposited. As illustrated in Fig.3, a photosresit layer is coated and defined to expose the pillar area. Copper and solder material (Sn) are electroplated in the openings. After the photoresist stripping, the UBM is wet etched to isolate the pillars. The copper pillar bumps are formed after reflow to a height of 13.5 μm and a diameter of 30 μm. The top view of the fabricated copper pillar bumps together with RDL is shown in Fig.4.

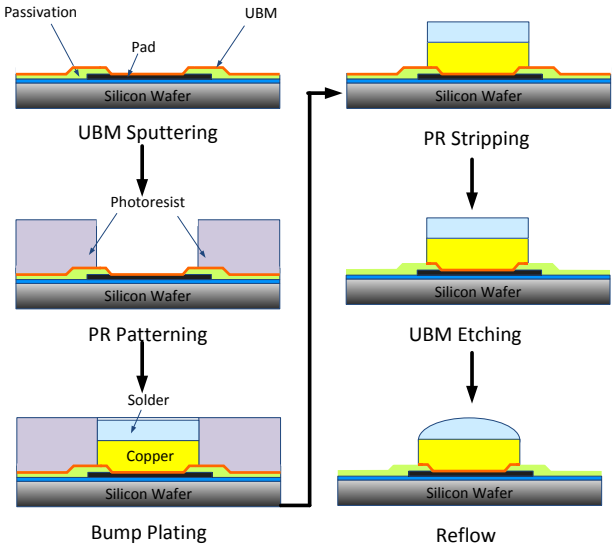

Fig.3 Process flow for fine pitch copper pillar bumps

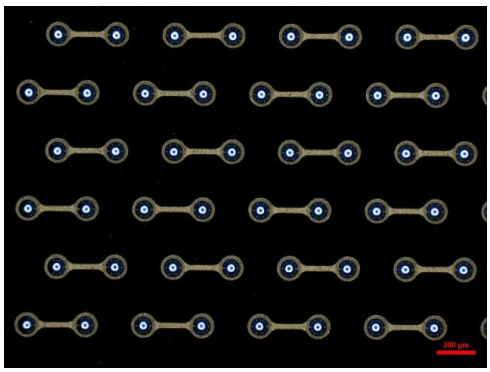

Fig.4 Optical picture of fabricated copper pillar bumps

B. Temporary bonding and wafer thinning

In this paper, we focus on the high temperature debonding method provided by Brewer Science. A glass wafer is selected as carrier, or handler wafer, for ease of observation of bonding defect. To achieve void free bonding, it is necessary to start with clean surfaces and to control the TTV of the adhesive layer. Prior to bonding, the device wafers are subjected to a full cleaning process. The device wafers are plasma cleaned by Oxygen ashing and Argon sputtering for 6 min. The wafers are then stepped to a rinse cycle of DI water for 10 min. This is followed by isopropyl alcohol (IPA) spin clean at 900 rpm.

After cleaning, the wafers are baked at 200℃ for 5 min. The carrier wafers are cleaned in two steps. Firstly, they are spin-cleaned with the WaferBOND Remover from Brewer Science at 900 rpm. Secondly, they are spin-cleaned with IPA at the same speed. The carriers are baked at 200℃ for 5 min. After cleaning, the device wafers are coated with the temporary bonding polymer, WaferBOND HT-10.10, at 900 rpm for 30 s. The coated device wafers are baked in two steps on a hot-plate, first at 120 ℃ for 2 min, followed by 180 ℃ for 2 min. No bubble formation is observed after the baking. The coated polymer is measured to be 27μm thick, which is twice the height of the copper pillar bumps. The surface profile is flat after the polymer coating on bumps, as shown in Fig.5. The carrier and silicon wafer pair is vacuum bonded by wafer bonder EVG 520 at 190 ℃ and with applied force of 3500N for 5 min. Fig.6(a) shows a magnified portion of a successfully bonded interface without bubbles when looking from glass carrier side. Large bubble are observed when the bonding surfaces have not been properly treated by above steps, as shown in Fig.6(b).

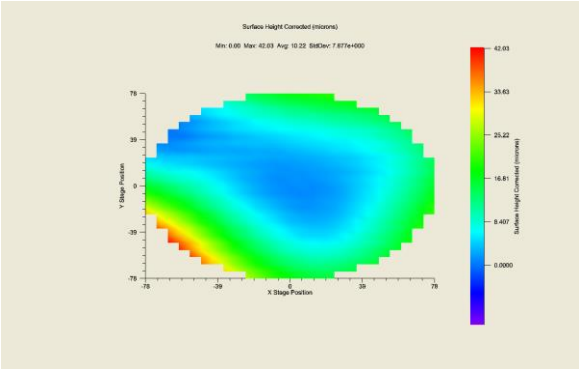

Fig.5 TTV of the coated bonding adhesives on a pillar bump wafer

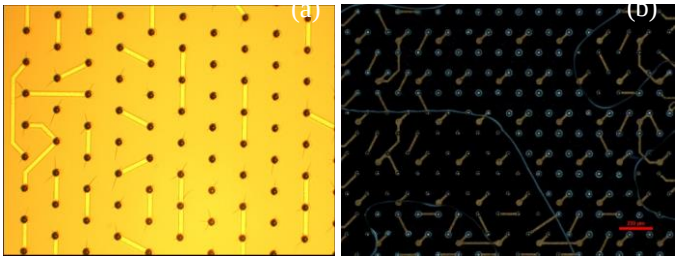

Fig.6 Optical pictures of (a) bubble free bonding and (b) bonding with visible bubbles

The back-side of the device wafers is ground to remove a thickness of about 550μm. To relieve the residual stress and micro-cracks resulting from the grinding process, the remaining 30 μm of silicon are removed by the deep reactive ion etching (DRIE). The surface conditions before and after DRIE etching is shown in Fig.7.

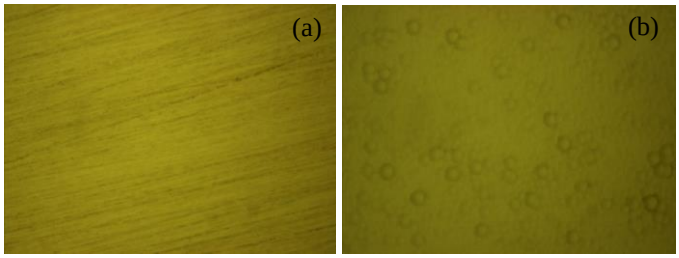

Fig.7 Wafer surface after (a) fine grinding and (b) dry etching

C. Debonding

After wafer thinning, the bonded pair is heated to 190 ℃ and slide debonded.by semi-automatic benchtop debonder *Cee 1300DB* from Brewer Science Inc.. In Fig.8 is shown a successfully debonded wafer.

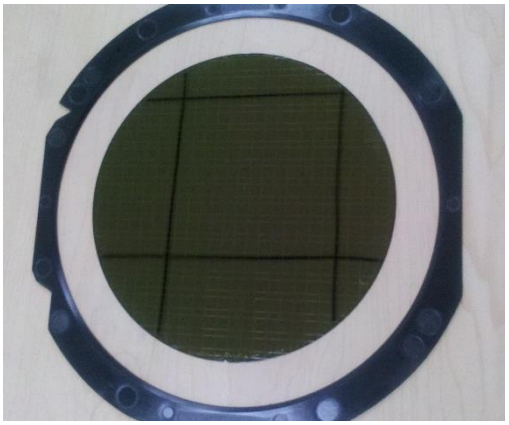

Fig.8 A successfully thermo-debonded wafer

IV. SUMMARY

This paper reports our process development on wafer temporary bonding, thinning and debonding for the TSV back-side process. The effect of thermal sliding on copper pillar bumps are simulated for different thermal bonding adhesive thickness. The TSV, RDL and fine pitch copper pillar bumps are fabricated on 8-inch silicon wafer. By a combination of meticulous application of wafer cleaning and optimization of bonding parameters, a void free bonding interface is achieved, which is sufficient to endure backside processes. The bonded wafer pair is successfully debonded by the application of a thermal sliding mechanism without breakage.

ACKNOWLEDGMENT

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