Effect of annealing after copper plating on the pumping behavior of through silicon vias

Liang Ji,Xiangmeng Jing,Kai Xue,Cheng Xu,Hongwen he,Wenqi Zhang
National Center for Advanced Packaging
NCAP
Wuxi, China
Liangji@ncap.com

***Abstract*—Though Silicon Vias(TSVs) are regarded as a key technology to achieve three dimensional(3D) integrated circuit(IC) functionality. Annealing a silicon device with TSVs may cause high stress and cause TSV protrusion because of high Coefficient of Thermal Expansion(CTE) between silicon substrate and TSVs. The TSV wafers could be annealed right after copper plating process, or after chemical mechanical polish (CMP) process, or both. In this paper, we report our research progress on the effect of annealing right after copper plating on the pumping behavior at different temperatures. Then the copper overburden is removed by CMP. The TSV wafers are tested at different temperatures for 30 minutes, 250℃, 300℃, 350℃, 400℃, 450℃, respectively. The pumping is measured by optical profiler, BRUKER Contour GT-X3. The finite element analysis method, ANSYS, is used to model and simulate the copper pumping at different temperatures. The pumping results with annealing at different temperatures are compared with those without annealing. It reveals that the pumping with annealing is larger than that without annealing. This is possibly due to higher level of stress release and microstructure evolution.**

Keywords—interposer ； though silicon via （tsv）； annealing；chemical mechanical polishing（CMP）;pumping；simulation;

I. INTRODUCTION

In recent years, Three-dimensional (3D) integration with through-silicon vias (TSVs) has emerged as an effective solution to decrease the length of chip interconnection, improve systems performance and reduce system power consumption.[1] A typical TSV process consists in etching the vias, protecting the sidewalls with insulation by CVD and depositing barrier and seed layer by PVD, then filling up the TSVs with a conductive material. For this filling several materials can be used, such as poly-crystalline Si or W, but in general Cu is preferred because of its optimal electrical conductive properties, ease of processing and reliability. However, The coefficient of thermal expansion (CTE) of Cu is much higher (16.7 ppm/℃)than the one of Si (2.3 ppm/℃). As a result，thermal expansion mismatch between copper (Cu) TSVs and silicon (Si) substrate can induce thermal stresses to cause TSV protrusion and interfacial delamination.[2-5] Thermo-mechanical reliability is a highly important reliability concerns, because process conditions during subsequent RDL ,bumping and die-stacking processes subject the wafers to repeated thermal loadings. So the thermal-mechanical stress can be accumulated during the process flow as RDL ,bumping, temporary bonding after TSV plating. It will cause fatal problems such as cracking, delaminating and voiding, If the thermal-mechanical stress don't release enough during annealing process after TSV copper plating. In addition, the interface of TSV between the copper and the silicon substrate will be delaminated because of the shear stress during thermal circle. Another reliability problem is the TSV protrusion problem. During subsequent fabrication processes, Cu TSVs were found to protrude out of the Si wafer surface due to high CTE between silicon substrate and TSVs, it can cause fracture of the dielectric materials upon TSVs. [6-8] In fact, The TSV wafers could be annealed right after copper plating process, or after chemical mechanical polish (CMP) process, or both. The stress might be thoroughly released by repeating annealing and CMP processes several times, however, the cost for fabricating the TSVs is increasing drastically, which is mainly attributed to the use of expensive CMP. To lower down the cost and minimize the CMP steps is one of the concerns from industry.[9]

In our study, the TSV diameter and depth are 20 μm and 100 μm based on 200mm wafer respectively. the correspond aspect ratio is 1:5. The material of sidewall insulation is SiO_2 deposited by PECVD, the barrier layer using physically vapor deposited (PVD) based material Ti. In fact, the material and thickness of insulation and barrier will also affect TSV protrusion. The influencing factors of copper protrusion is multifactorial not only related to annealing temperature but also related to material of sidewall and barrier. Therefore, the release of TSV stress and improve reliability for back-end-of-line (BEOL) is a comprehensive work, we need to study the various factors as annealing condition, materials of sidewall and barrier and the chemistry of copper plating solution in order to get better result. In this paper, we focus on the protruding results with annealing at different temperatures compared with those without annealing. The preliminary results show that the annealing after copper plating process affects the TSV microstructure evolution and pumping of TSVs. The pumping and TSV microstructure with annealing is larger than that without annealing.

II. TEST VEHICLE FABRICATION

Before the experiment, several samples have been prepared for the test.

The process flow of TSV fabrication is illustrated in Figure 1: (a) the process start with a 200mm and double polished

blank wafer. (b) the vias etching use Deep Reactive Ion Etch (DRIE) because of the high etching efficiency. The via size is 20 μ m in diameter and 100 μ m in depth respectively. (c) after the via etching, we have to deposit the insulation material on the silicon surface and over the sidewall. This is a very important process for TSV fabrication, because silicon substrate is semiconductor which generate large leakage current without insulation overburden when used in high speed interconnection. In this case, the insulation layer SiO_2 is deposited by PECVD.(d) after insulation depositing, we need to fill TSVs with copper. Firstly, we have to deposit barrier layer using PVD in order to prevent copper ions in TSV diffuses to silicon substrate, we use Ti as the barrier material in this flow. Secondly, we deposit copper seed layer by PVD for the later plating. Finally，The vias are filled with copper by plating, the overburden upon silicon is about 5 μ m (e) then the wafers are annealed at 350℃ for 30 minutes.(f) the copper overburden is removed by CMP.(g) The TSV wafers are tested at different temperatures, 250℃, 300℃, 350℃, 400℃, 450℃, respectively. The protrusion is measured by optical profiler, BRUKER ContourGT-X3. Figure 2 illustrate the cross section and array of TSVs, there is no defect inside TSVs.

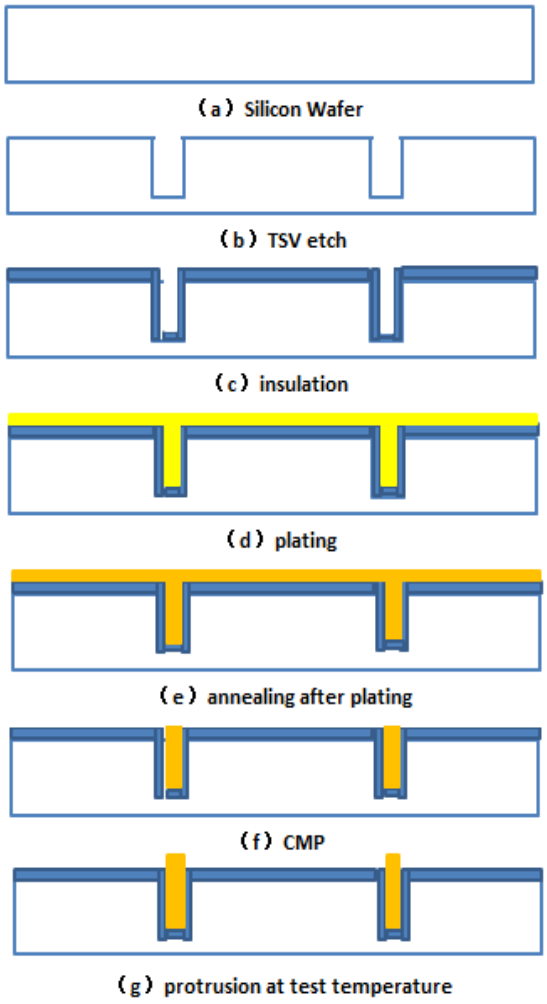

Figure 1 process flow of TSV fabrication

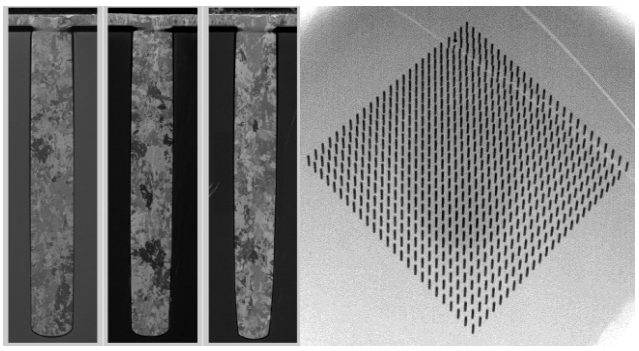

Figure 2 cross section and arrays of TSVs

III. THERMAL STRESS MODELING AND SIMULATION

The finite element method (FEM) is used to model and simulate the thermal stress and mechanical behavior of TSV after the annealing condition. By using ANSYS, We model a single TSV with 20μm in diameter and 100μm in depth, covered by 300 nm SiO_2 liner as insulation and (100) silicon substrate . The key simulation parameter Settings are as follows: The thermal expansion coefficient of silicon is 17.3(ppm/k) and the thermal expansion coefficient of silicon is 3.3(ppm/k), the thickness of silicon is 700 μ m. The simulation result of the cross section after annealing is showed in figure 3.

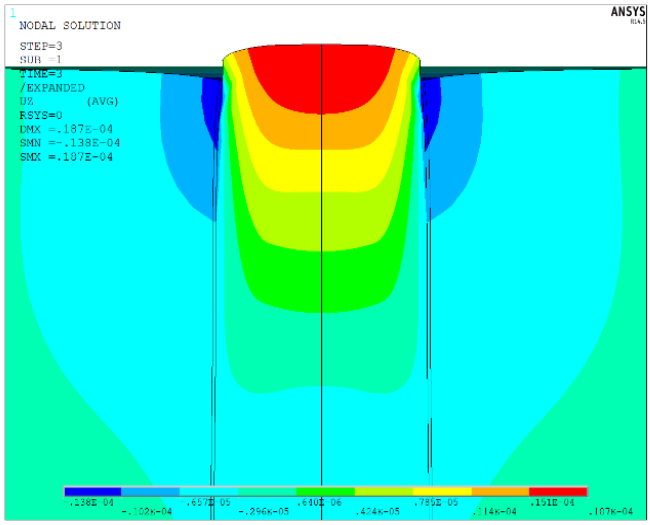

Figure 3 the simulation result of TSV protrusion

In figure 3, we can observe the TSV protrusion and stress distribution obviously. Due to the CTE mismatch between silicon substrate and TSV, the maximum stress occurs at the top of the copper via and reduces with the distance to the top. We can also see that the minimum stress occurs at the silicon close to the edge of copper via. The stress and protrusion will be harmful to the reliability of 2.5D/3D device.

The simulation also include various annealing temperature from room temperature to 450 ℃. The copper protrusion height of different temperature is showed in figure 4.

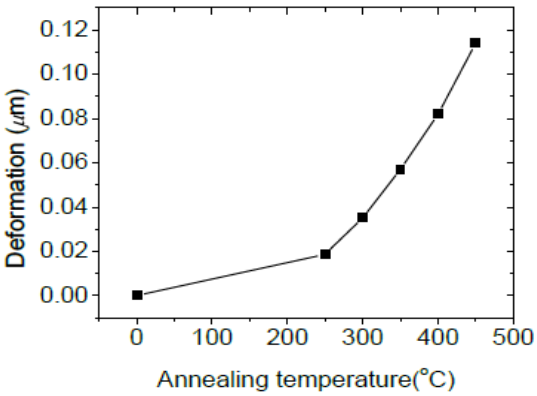

Figure 4 copper protrusion at different temperature

In figure 4, the copper protrusion height increase with the increase of temperature. We can notice that the protrusion height increase slowly under 250℃, when the annealing temperature above 250℃,it increase dramatically. In order to get enough stress release for TSV, we need to set the annealing temperature point above 250℃. In this case, the annealing temperature point is set around 350 ℃.

IV. RESULT AND DISCUSSION

The protrusion of TSV is measured by optical profiler, BRUKER Contour GT-X3. A typical TSV profile which annealed at different temperature is illustrated in figure 5.

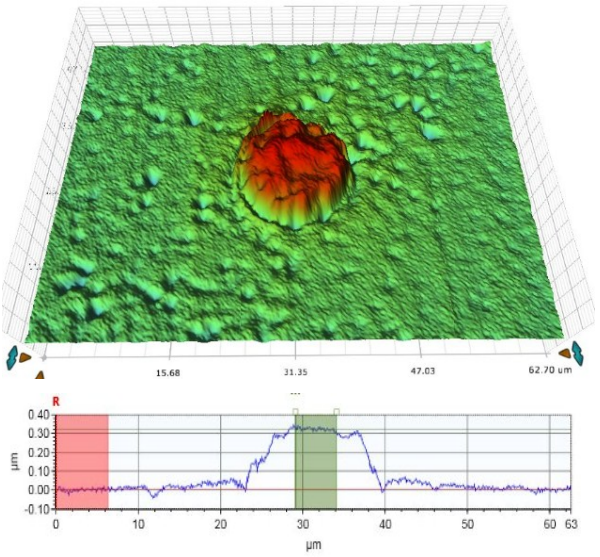

Figure 5 profile of TSV annealed at 300℃

In figure 5, the height of TSV protrusion is bigger than the simulation result. This is mainly due to the thermal simulation can not contain the effects of chemical plating solution, TSV scollops, dielectric layer material and other factors. As we know, TSV protrusion is a complex phenomenon which contains a variety of influencing factors, it is hard to make a accurate simulation. In fact, the purpose of thermal simulation is to find the protrusion trend at different temperature. There is a small dishing at the edge of TSV, this is because of the effect of shear stress between silicon substrate and copper via. It will cause cracking between silicon substrate and copper via if the shear stress is too big.

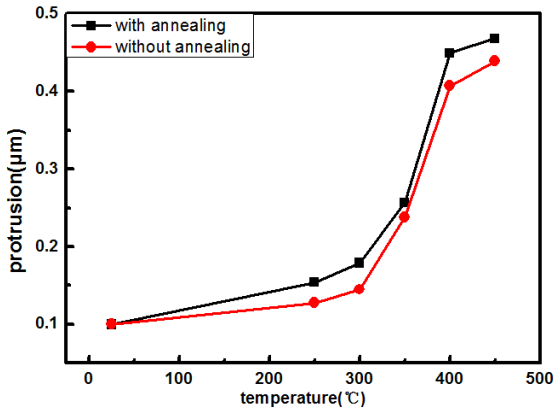

Figure 6 copper protrusion at different temperature by test

In figure 6, the protrusion trend at different temperature is similar to the simulation result. The height of TSV protrusion increase fast above 300℃. Therefore, the thermal mechanical simulation have some guidance for the TSV annealing experiment. Comparing the two different curve, we can notice that the two curve are almost coincident under 400℃. At 450℃, the height of TSV with annealing is a bit higher than that without annealing. But overall, we consider that annealing has little effect on TSV protrusion in this case.

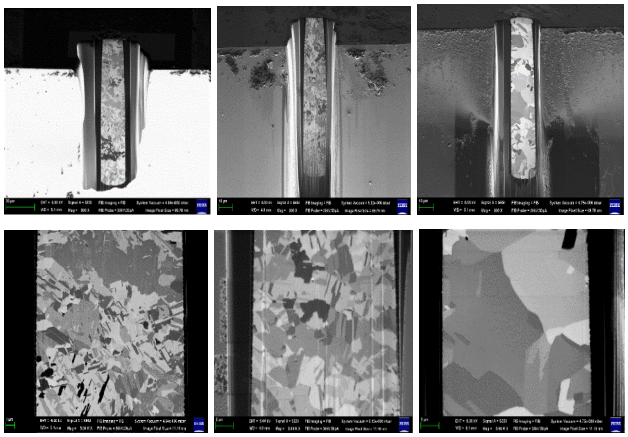

Figure 7 SEM of TSV without annealing at different test temperature

The cross section of TSVs are illustrated in figure 7 by FIB and SEM, it is obvious that the copper crystal structure is much larger than another two in the picture. Therefore during the test process at 450 ℃ for 30min, the copper crystal structure is growing much fast and the stress in TSVs is released sufficiently. As a result, according to figure 4, we can notice that the height of TSV protrusion at 450℃ is dramatic higher than others. It increase hugely under the test temperature from 350 ℃ to 450 ℃. The increment of the pumping is about 0.25 μ m. however, the size of copper crystal

structure at test temperature with 350℃ is similar to that without heat treatment. According to figure 6, The increment of the TSV pumping is about 0.08μm by the test temperature from 25℃ to 350℃, it is much smaller. In this case, the annealing temperature set at 350℃ for 30 minutes，based on the comparing of pumping height and copper crystal structure from room temperature to 350℃，respectively, we can conclude that the stress in TSV is not released enough under annealing temperature of 350℃. therefore the two curves in figure 6 perform same trend from room temperature to 450℃. According to TSV protrusion profile and copper crystal structure in figure 5 and figure 7, we conclude that the 350℃ annealing have a little help to release thermal stress in this case. But at 450℃ annealing, the stress release much more.

V. CONCLUSION

In this paper, we fabricate TSV test vehicle by our process flow. The TSV size is 20μm width and 100μm depth, the overburden upon silicon substrate is about 5μm. Annealing temperature set at 350℃ for 30 minute, after that the overburden is removed by CMP, finally we test the height of protrusion and copper crystal structure at 250℃, 300℃, 350℃, 400℃, 450℃ for 30 minute, respectively.

According to the experiment and test result, the height of protrusion and copper crystal structure with annealing are similar to those without annealing. The stress release not enough at 350℃ for 30 minute. In order to solve the problem, some solutions will be test for further experiments.

1) Improving annealing temperature: According to the experiment, we see that the stress release enough at 450℃ annealing. However 450℃ annealing maybe too high for active device, it will lead to device failure. But for passive device such as interposer, 450℃ annealing is tolerable. Annealing temperature 420℃ is used in IMEC's TSV process flow.[10]

2) Removing overburden before annealing by CMP: according to P. Saettler's research[11], the stress inside TSV release sufficiently without overburden. However we do not want to do a CMP before annealing because of the high cost of CMP. A better method is to improve plating process to reduce overburden thickness.

3) Improving EP chemistry to optimize copper protrusion according to Jinho An'work. TSV protrusion can be controlled by different EP chemistries, as well as different anneal temperature that affect stresses at the isolation oxide layer and the thermal stabilization of the TSV for identical temperature anneal conditions.[12]

Acknowledgement

The research funding from China National Science Foundation with contract No. 61204115 and National S&T Major Project with the contract No. 2013ZX02051 is greatly acknowledged.

References

[1] Holger Roth, Zhenhui He, Thomas Mayer, "Inspection of Through Silicon Vias (TSV) and other Interconnections in IC packages by Computed Tomography," 11th Electronics Packaging Technology Conference, Singapore 2009.

[2] Chukwudi Okoro, Kris Vanstreels, Riet Labie, "Influence of annealing conditions on the mechanical and microstructural behavior of electroplated Cu-TSV", JOURNAL OF MICROMECHANICS AND MICROENGINEERING, J. Micromech. Microeng. **20** (2010) 045032 (6pp).

[3] Lu, K. H. et al, "Thermo-Mechanical Reliability of 3-D ICs containing Through Silicon Vias," Proc 59th Electronic Components and Technology Conf, San Diego, CA, May 2009, pp. 630-634.

[4] W.S.Kwon, D.T.Alastair,K.H.Teo, "Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy". APPLIED PHYSICS LETTERS 98, 232106 （2011）

[5] L. Kong, A. Rudack, P. Krueger, H. Zschech, S. Arkalgud, A. Diebold, "3D-interconnect: Visualization of extrusion and voids induced in copper-filled through-silicon vias (TSVs) at various temperatures using X-ray microscopy", Microelectronic Engineering, 2011.

[6] T. C. Tsai, W. C. Tsao, W. Lin, C. L. Hsu, C. L. Lin, C.M. Hsu, et al., "CMP process development for the via-middle 3D TSV applications at 28 nm technology node", Microelectronic Engineering, 2011..

[7] Dixit P ,"Characterization of nano-grained high aspect ratio through-wafer copper interconnect column". ECTC Conf. (Reno, NV, USA) pp 2011–6.

[8] Karmarkar AP, Xu X, Moroz V. "Performance and reliability analysis of 2Dintegration structures employing through silicon via (TSV)". In: Proc IEEE 47.Annual Int Reliab Phys Symp; 2009. pp. 682–7.

[9] Zhao hui, c., S. Xiaohui, et al. "Thermo-mechanical characterization of copper filled and polymer filled tsvs considering nonlinear material behaviors", Electronic Components and Technology Conference (2009).

[10] Xiangmeng Jing, Hongwen He, Liang Ji, "Effect of Thermal Annealing on TSV Cu Protrusion and Local Stress", Electronic Components and Technology Conf, May2013, pp. 461-466.

[11] P. Saettler, D. Kovalenko, K. Meier, "Thermo-mechanical Characterization and Modeling of TSV Annealing Behavior", 2012 13th international Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems, EuroSimE 2012.

[12] Jinho An, Kwang , Jin Moon, "Annealing Process and Structural Considerations in Controlling Extrusion-type Defects Cu TSV". IEEE International Reliability Physics Symposium , April 2011, 3D.1.1-3D.1.7.