Modeling, Simulation and Analysis of Coplanar Waveguide on Glass Substrate for 2.5D Integration

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***Abstract*—Glass is an ideal material for 2.5D packaging application with excellent electrical, optical and mechanical properties. In this paper, several forms of coplanar waveguide (CPW) on glass substrate were modeled and simulated using 3D full-wave finite element method (FEM). The target of this research was to provide guidance for the design and analysis of CPW on glass substrate. Analyses of CPWs on different redistribution layers (RDLs) with various line lengths are presented. And the comparison of the performances of CPWs on silicon substrate and glass substrate are also described in this paper. The simulation results illustrate the electrical performances of CPWs on glass substrate are much better than on silicon substrate, especially in high frequency range.**

Keywords—Coplanar Waveguide (CPW); Glass Substrate; Finite Element Method ; transmission characteristic

I. INTRODUCTION

In the field of advanced package, glass has won more and more attention with various advantages. Currently, ceramic substrate owns the best electrical performance in high frequency range, but its widespread applications are limited by low wiring density. Also, the widely used organic substrate has the disadvantage of poor CTE match with silicon chips. Newly developed silicon interposer is challenged by high electrical loss and high process cost. Compared with the materials mentioned above, glass substrate has the advantages of excellent insulating property, large panel availability and good CTE match with silicon. Then, glass substrate could support short interconnects and high wiring density in low cost packaging applications. However, one of the manufacturing issues of glass via formation is a big obstacle for its wide application.

Coplanar Waveguide（CPW） has many advantages over conventional microstrip lines, such as its simple fabrication process, less radiation loss, small form factor and so on. A conventional CPW on a dielectric consists of a center strip conductor and semi-infinite ground planes on either side as shown in Fig.1. As the signal line in CPW structure is unwrapped, the electrical characteristics of dielectric substrate affect CPW's performance greatly. CPW is widely used in scale-limited 2.5D package with its unique advantages. Therefore, the simulation and optimization of CPW on glass are important topics for advanced package designs.

In this research, we first introduced the structure of the redistribution layers designed on glass substrate, which constitute the main body of CPWs. Then, analysis of electrical performances of CPWs on different redistribution layers was carried out. After that, the effect of line lengths on CPWs electrical performance was studied. At last, electrical characteristics of CPWs on silicon and glass substrate were compared.

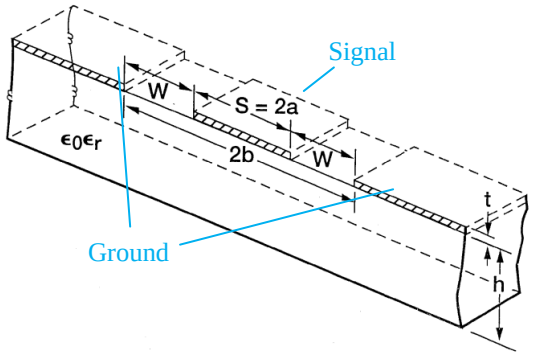


Fig.1. Schematic view of conventional coplanar waveguide

II. MOLDING AND SIMULATION PROCEDURE

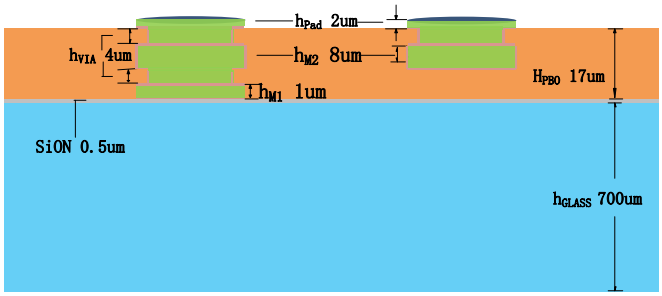


Fig.2. Cross-section view of the CPW models

The cross-section view of the CPW models included two redistribution layers is illustrated in Fig.2. Dimensional parameters and material parameters of these models are provided respectively in Table 1 and Table 2. A glass wafer with thickness of 700μm was prepared for the experiment. SiON (silicon oxynitride) film was deposited on the wafer for

light shading when photolithography is performing. In the following metallization process, two metal layers were formed by electroplating. Then，polymer was coated on these metal layers. Finally, pads were connected to the top metal for package and test.

Table 1 Dimensional parameters

Dimensional Parameters	**Typical Values (μm)**
Height of Glass wafer (h_{Glass})	700
Thickness of First RDL (h_{M1})	1
Thickness of Second RDL (h_{M2})	8
Height of Via（h_{VIA}）	4
Side Length of VIA（l_{via}）	100
Height of Pad (h_{Pad})	2
Side Length of Pad (h_{Pad})	115
PBO Thickness(h_{PBO})	17

Table 2 Material parameters

Material Parameters	**Typical Values**
Bulk Conductivity of Cu （$\sigma_{Cu}/(S\bullet m^{-1})$）	5.8 x10^7
Relative Permeability of Cu (μ_{cu})	0.9999991
Relative Permittivity of Glass Wafer ($\varepsilon_{r,\ glass}$)	4.6
Dielectric Loss Tangent of Glass ($\tan\delta$)	0.0037
Relative Permittivity of PBO （$\varepsilon_{r,PBO}$）	2.94

A. Analysis of electrical performances of CPWs on different redistribution layers

The model of CPW on glass substrate is illustrated in Fig.3. We set the models showed in Fig.3 same with line width, pitch and length，but different with redistribution layers (M1/M2). Fig.4 shows the simulation result of these models.

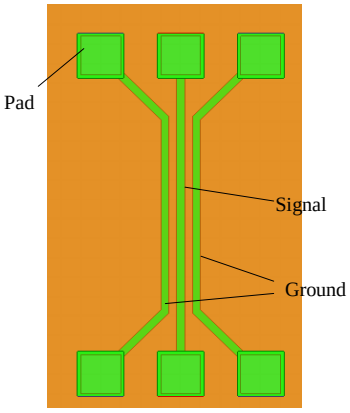


Fig.3. Model of CPW in HFSS

Fig.4 illustrates that the performance of CPW on M2 is much better than the one on M1. As glass has little substrate losses, the thickness of metal layer affect the electrical performances of CPWs greatly. Limited on process fabrication technology, the lower metal layer on glass is much thinner than the upper layer. The thickness of the metal layer influences the characteristic impedance and the characteristic impedance affects the performance of the transmission line. So in the high dense package application, the amount of transmission lines on M1 should be limited.

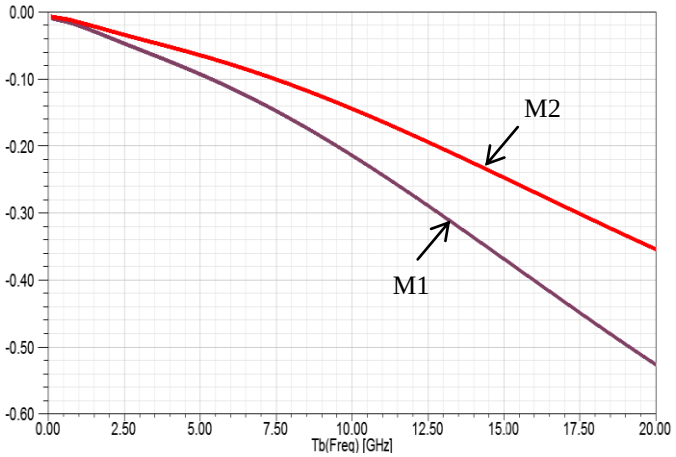


Fig.4. S21 of CPW on different redistribution layers

B. Study of line lengths on CPWs' electrical performance

Insertion loss of CPWs with different line lengths were compared in Fig.5. The CPWs were built on the same metal layer, with same line width and pitch. Fig.5 shows that S21 value increases greatly with the increasing of line length. When the line is over 2000μm, resonance oscillation occurs. Inductive effect increased with the growth of line length. Therefore, in high speed and high power consumption systems, long transmission lines should be avoided.

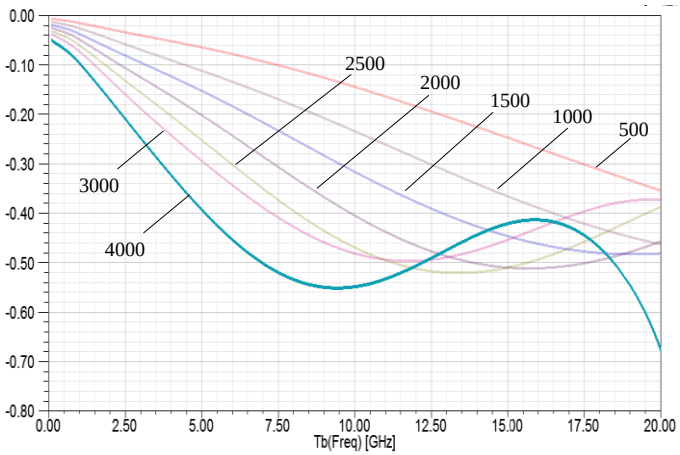


Fig.5. S21 of CPWs with different line lengths

III. COMPARATION OF CPWS ON GLASS AND SILICON SUBSTRATE

In this section, CPWs in the same dimensions were built on the glass substrate and silicon substrate respectively. The

parameters of silicon substrate we chose are illustrated in Table.3. The structure of RDL on silicon substrate is identical to the one on glass substrate. In the fabrication process of the silicon wafer, an insulating layer（SiO_2）with thickness of 2μm is covered on its surface. Fig.6 shows the CPW models on silicon substrate in HFSS.

Table 3 material parameters of silicon substrate

Material Parameters	Typical Values
Bulk Conductivity of Silicon （$\sigma_{Si}/(S\bullet m^{-1})$）	10
Relative Permittivity of Silicon Wafer ($\varepsilon_{r,\ silicon}$)	11.9
Dielectric Loss Tangent of Silicon ($\tan\delta$)	0.04
Relative Permittivity of Silicon Dioxide（ε_{r,SiO_2}）	4

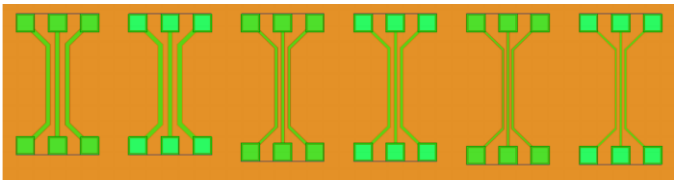
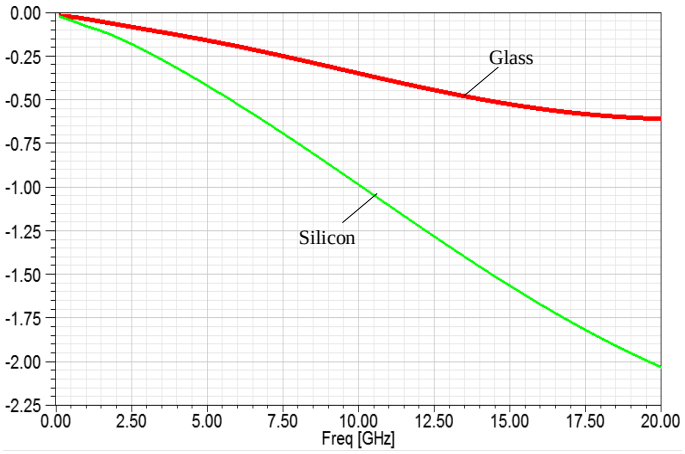


Fig.6. Models of CPWs on silicon substrate in HFSS

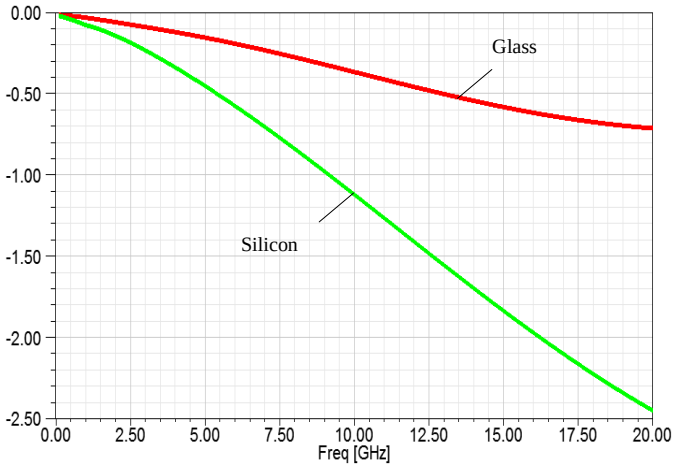
A. Comparison of insertion loss of CPWs on glass and silicon substrate

Limited by processing technics, the minimal line width and line pitch of RDL are usually in the same. The models we built also follow this rule. The CPWs we compared on silicon and glass substrate are in the same length of 1000um with different line width of 15μm, 20μm and 30μm. The results of the comparison of insertion loss are showed in Fig.7.

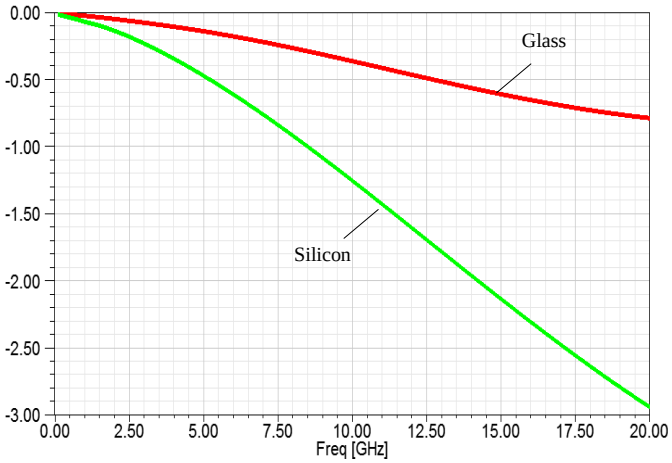
Fig.7 indicates that CPWs on glass substrate have much better electrical characteristics than on silicon, especially in higher frequency range. When the frequency is over 12.5GHz, the difference between two curves is over 1dB. Because of specific material property of silicon wafer, transmission lines got extra substrate loss from silicon. As signals went through signal lines, coupling structures generated between copper line, SiO_2 insulating layer and silicon substrate. That's increased power consumption on signal lines and increased the insertion loss. In contrast, little substrate loss exists in glass substrate. The insertion loss on glass comes mainly from the conductor loss of copper line. With advantageous properties, glass wafer could be a perfect candidate for 2.D package application.



(a) Line width and line pitch in 15μm



(b) Line width and line pitch in 20μm



(c) Line width and line pitch in 30μm

Fig.7. Comparison of insertion loss of CPWs on glass and silicon substrate

B. *Comparison of characteristic impedance of CPWs on glass and silicon substrate*

In this part, we focused on the study of characteristic impedance of transmission lines on different substrates. Two models in the same length of 1000μm and same line width of 20μm are chosen for the comparison. The results of characteristic impedances of CPWs on glass and silicon substrate were illustrated in Fig.8.

Fig.8 shows the curve of silicon is lower than that of glass. Four primary factors influence characteristic impedance of transmission lines on different substrates. They're line width, thickness of conductor, thickness of packaging material and relative permittivity of substrate material. In this case, effect of relative permittivity (ε_r) of substrate plays a leading role. Obviously, relative permittivity of silicon substrate is much higher than glass substrate. Lager permittivity brings higher capacitance per unit length of transmission lines, and lager capacitance leads to lower characteristic impedance.

In practical application, 50Ohm is usually acquired for impedance matching. The data above shows that glass substrate have better properties than silicon substrate under the same wiring dense. Therefore, application of glass substrate could save more wiring area than silicon substrate.

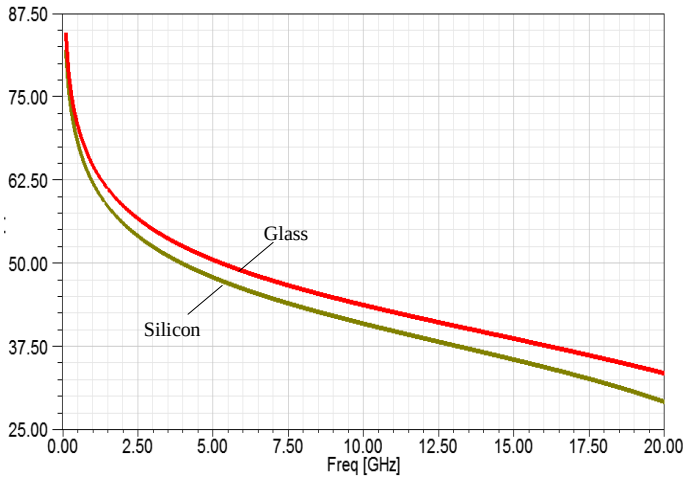


Fig.8 Comparison of insertion loss of CPWs on glass and silicon substrate

IV. CONCLUSIONS

In this paper, we studied the electrical performances of coplanar waveguide on glass substrate. Based on the process commonly used, CPWs on different redistribution layers and in various line lengths were modeled and simulated. Performances of CPWs in different line width and line pitch on glass and silicon substrate were compared. The results show great differences in transmission performance with various conditions, especially in high frequency range. Transmission lines on glass substrate not only have much lower consumption, but also could be built into higher wiring dense.

ACKNOWLEDGMENT

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