Electrical Simulation of Thin Film Inductors on Silicon and Glass Substrates

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***Abstract*—Passive devices are widely used in all kinds of systems. Generally, most of the passive components in an electronic system are assembled as discrete components or passive arrays. But a discrete passive component occupies a lot of space for the realization of its function. To overcome this shortcoming, one promising way is the integration of passive components into system in package. In this paper, we designed two kinds of thin film spiral inductors on both silicon and glass substrates. One is monolayer structure and, another has double layers. The inductors were modeled and simulated using Finite Element Method (FEM). And, the electrical analysis was performed by ANSYS HFSS and Q3D.**

Keywords—thin film, electronic packaging technology, passive component, glass substrate, thin film spiral inductor

I. INTRODUCTION

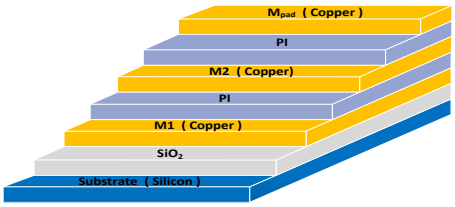
Today most of the passive components required in an electronic system are assembled as discrete components or passive arrays. Such components offer broad value ranges for all passive types as well as tight tolerances and availability in different package sizes. But in relation to an IC with a very high integration density a discrete passive component requires a lot of space for the realization of its single inductive, capacitive or resistive function. For systems using a large number of passives would lead to an additional need for board area comparable to the area consumed by the active devices. But beside the area consumption aspects like parasitic influences, caused by long feedings and solder connections, reduced assembly yield caused by abundant solder joints as well as high assembly costs caused by long placement times can be disadvantageous for the realization of future electronic systems [5,6,7]. Especially products in the "hand held" as well as in the "high performance" sector are indicated to be affected by these disadvantages. Thus these products are the driving force for new technologies overcoming the drawbacks of discrete passives [1]. For further miniaturization and high-density growth, it is necessary to integrate passive components into thin film multi layer systems. With this approach multi chip module substrates (MCM-D) or integrated passive devices (IPDs) can be realized with passive elements having high accuracy and high density.

In recent years, the thin film passive elements have been studied extensively. Most of the researches are focus on the passive device such as balun, filter, diplexer, divider etc. But the best performance of the passive device will always be obtained with passive inductors and capacitors. Unfortunately, standard integrated circuit technology has not evolved with a focus on providing good passive elements. So people try to find out some important parameters which will affect the performance of the passive element. Since design parameters for resistors and capacitors can be easily calculated, in this study inductors were chosen to be simulated. Although the using of silicon substrates can solve most of these issues, silicon has shortcomings such as high electrical loss and high cost. While glass substrate is a good candidate for short interconnects and high wiring density [1]. As compared with silicon, glass substrate has great advantage in high frequency range due to its low loss property. The glass interposer provides less substrate coupling and the IPDs on glass can achieve higher quality factor (Q-factor). Moreover, glass substrate can be a low cost packaging solution due to its low price and large panel processing compatibility. However, the issue of glass etching especially for wires with fine width and vias with high aspect ratios can be a great obstacle for its wide application [2].We designed the inductors on both silicon and glass substrates in this paper. First we will give a shout introduction of the laminate structure and the design parameters of thin film inductors. Then the performance of the inductors on both silicon and glass substrates will be compared. At last the results of present work were summarized in this paper.

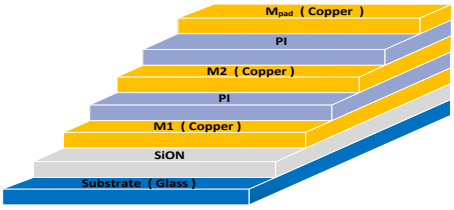
II. THIN FILM BUILD-UP AND FABRICATION OF MULTILEVEL METAL LAYERS ON SILICON AND GLASS WAFER

A. Thin Film Build-up

Fig. 1 shows the construction of thin films for the integration of inductors. The top metal layer represents the pad. For cost point of view, planar spirals are the preferable structures for the realization of integrated inductors in thin film technology. With this approach only two metal layers are needed. In case of a single layer coil conductor is formed to a spiral in one of the two metal layers. And the other metal layer is used to route the inner coil contact to the outside by using a simple underpass. In case of a double layer coil the two metal layers are both used to achieve a strong magnetic field coupling.



a. Inductors on silicon substrate



b. Inductors on glass substrate

Fig. 1. The building up of thin films for inductors

B. *Fabrication*

Fig. 2 gives the process flow we used for the fabrication of thin film inductors on silicon and glass. First, a wafer with thickness of 200μm is prepared. After wafer-cleaning, a SiO_2 (silicon dioxide) or SiON (silicon oxynitride) film is deposited on the wafer. To prevent substrate losses, SiO_2 was chosen as the insulation layer. And the SiON layer is dark, which can resist light leakage through glass wafer when photolithography is performing. Next, the first metal layer is deposited, followed with the polymer coating. And the upper metal layers are fabricated with the same procedure. Pads are finally connected to the top metal, which were used for package and test. In these processes, Ti is used as barrier layer to prevent copper's diffusion.

III. DESIGN OF INDUCTORS

Inductors can be realized in one of the following three forms: a small section of a strip conductor or a wire. The thin-film inductor is used for low inductance value, typically less than 2 nH and often meandered to reduce the component's size. Thin film single-loop inductors are not as popular as their coil versions due to their limited inductance per unit area [3]. Planar thin film inductors have a lot of different design parameters which are in form of the spiral (square, octagonal, Archimedes), number of layers, number of turns, coil area, line width, line pitch as well as line thickness. Because of the large variety of possibilities the form was not altered in this work and fixed to the octagonal type for study examples. Design parameters are shown in Fig. 2, Fig. 3 and TABLE I. Two kinds of M2 with height of 8μm and 20μm are designed to compare different performances. As shown in figure 3, the double layer inductor is designed with some vias to connect the two metal layers.

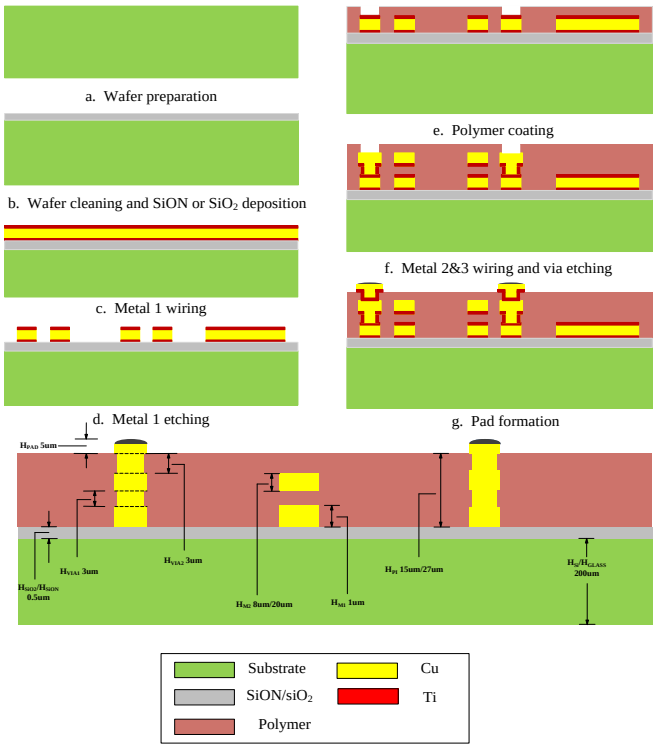
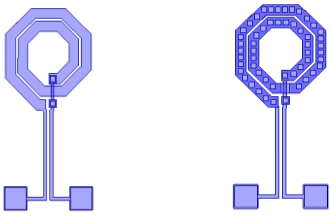


Fig. 2. Process flow for multilevel metal layers fabrication on glass and silicon wafer

Every inductors in this paper have an inside diameter of 250μm, outside diameter of about 520μm, 2 turns.

TABLE I. THE SIZES OF THE MODEL

Size Definition	Typical Values
Substrate Height（H_{Si} /H_{GLASS}）	200μm
Insulator(SiO_2/SiON) Thickness(H_{SiO2}/$H_{Si\ ON}$)	0.5μm
The First Metallic Layer(Cu) Thickness(H_{M1})	1μm
Via1 Height(H_{VIA1})	3μm
The Second Metallic Layer(Cu) Thickness(H_{M2})	8μm/20μm
Via2 Height(H_{VIA2})	3μm
Pad Height(H_{PAD})	5μm
PI Thickness(H_{PI})	15μm/27μm



a. Single-layer inductor b. Double-layer inductor

Fig. 3. Schematic view of the single-layer and double-layer

IV. Electrical Performance of Thin-film Inductors

A. Inductance L of Inductors with One and Two Metal Layers

In electrical circuits, the effect of magnetic energy storage is represented by an inductance L, which is defined in terms of magnetic flux ψ by

$$L = \frac{1}{I}\oint_S B \cdot ds = \frac{\Psi}{I}$$

$$= \mu_0 \mu_r \frac{1}{I}\oint_l H \cdot dl \qquad (1)$$

where I = the current flowing through the conductor in amperes, B = magnetic flux density expressed in tesla (T) or Wb/m^2 = $\mu_0 \mu_r H$, Where the magnetic field, H is expressed in amp/m, S = surface area enclosed by the loop of wire of length l. For perfect conductors $\mu_r = 1$. Free-space permeability is $\mu_0 = 4\pi \times 10^{-7}$ H/m. According to (1), although silicon and glass have different relative permittivity, it has no effect on the L, which is proved in Fig. 4. As shown in the simulation result (Fig. 4), no matter single layer or double layers, the L of the inductor will become lower when the metal layer becomes thicker. In view of the process, thick metal layer will introduce new problems, double-layer inductors come into the mainstream.

B. Quality Factor for Double-layer Inductors on Silicon and Glass Substrate

Fig. 5 shows the quality factor (Q-factor) for the inductors. Several different definitions of Q-factor for inductors have been used in different literatures. In this paper, Q-factor is expressed as

$$Q_{eff} = \frac{\mathrm{Im}[Z_{in}]}{\mathrm{Re}[Z_{in}]} = \frac{X}{R} = \frac{\omega L_e}{R} \qquad (2)$$

where $\mathrm{Re}[Z_{in}]$ and $\mathrm{Im}[Z_{in}]$ are the real and imaginary parts of the input impedance of the inductor, respectively. This definition leads to the unusual condition that Q_{eff} becomes zero at resonance. Since in RF and microwave circuits, for series applications of inductors, the operating frequencies are well below the self-resonance frequency, the preceding definition is traditionally accepted. According to the simulation result (Fig. 5), the Q-factor of the inductor on glass substrate is larger than its corresponding structure on silicon substrate above 1GHz (HM2=8μm) and 2GHz (HM2=20μm) respectively. And the gap becomes bigger with the increasing of frequency. This result indicates that glass devices have better electrical performances in RF applications especially at high frequencies.

C. Coupling Between Inductors

When two inductors are placed in proximity to each other, their EM fields interact and a fraction of the power present on the primary or main inductor is coupled to the secondary inductor, which is known as parasitic coupling. Parasitic coupling affects the electrical performance of the circuit in several ways. It may change the frequency response in terms of frequency range and bandwidth, and it may degrade the gain/insertion loss and its flatness, input and output VSWR, and many other characteristics including output power, power added efficiency, and noise figure depending on the type of circuit. The coupling can also result in instability of an amplifier circuit or create feedback that results in a peak or a dip in the measured gain response or make a substantial change in the response of a phase shifter. In general, this parasitic coupling is undesirable and is an impediment to obtaining an optimum solution in a circuit design [3].

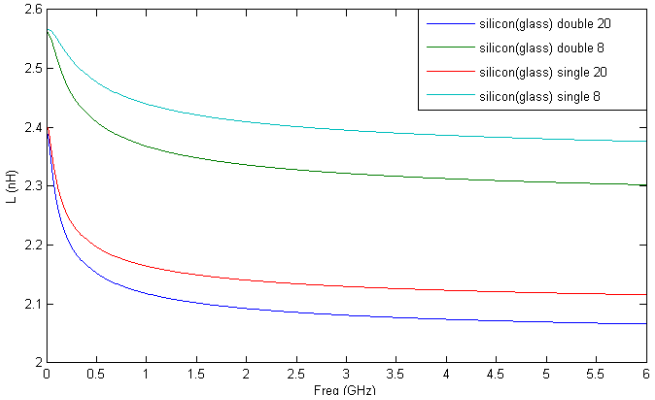


Fig. 4. Simulate L of inductors in silicon and glass substrates

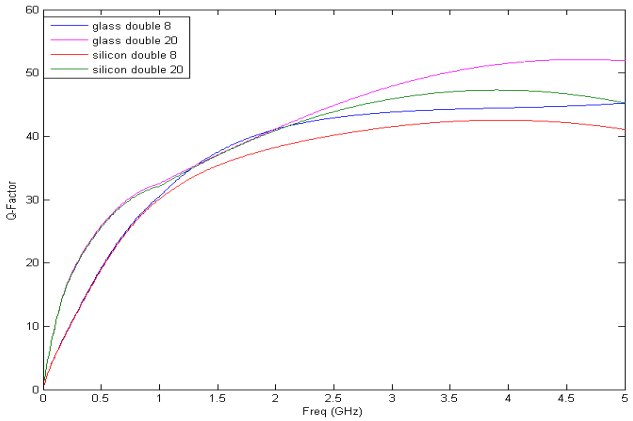


Fig. 5. Q-factor simulation result of the double-layer inductors

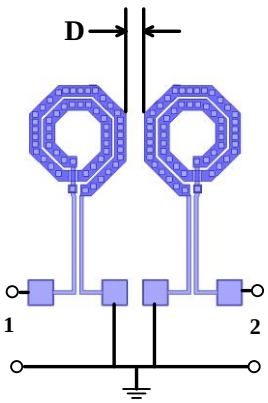


Fig. 6. Model for studying coupling

Fig. 6 shows the measured S_{21} response representing the coupling between two inductors. Fig. 7 shows the coupling of two inductors, between which the distance is 50μm. H8 means the height of the second metal layer is 8μm. In glass substrate, the resonance point frequency is higher than the inductor on silicon substrate, which means inductors have a better high frequency performance in glass substrate. With the increasing trend of electronic equipment working frequency and decreasing trend of costs, glass will be a better choice for being substrates.

As shown in Fig. 8, we simulate two inductors (HM2= 8μm and HM2=20μm) to find out the effect of the height of metal layer. Below 1.5 GHz, the height has little influence in coupling. But with the frequency increasing, the thinner the metal layer, the lower frequency the resonance point will be got. And below the resonance point, coupling of the thin metal layer inductors is much smaller.

Fig. 9 shows how distance between two inductors affects the coupling. The inductors are in glass substrate. As we know, long distance should reduce the coupling. But it also makes the resonance point move to low-frequency. In some radio equipment resonance may good for amplifying the weak signal. While in electronic power systems resonance should be avoid. So the balance of coupling and resonance point should be paid attention.

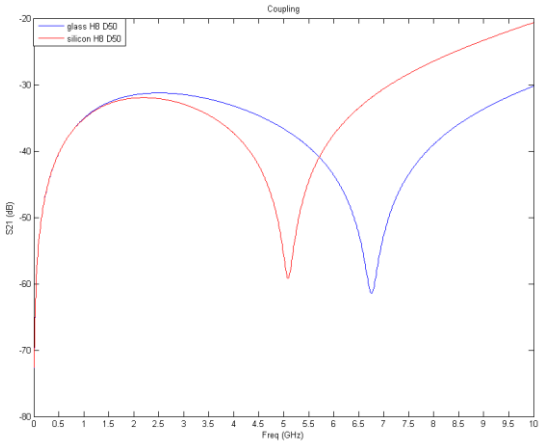


Fig. 7. Simulated response of two 50μm apart inductors

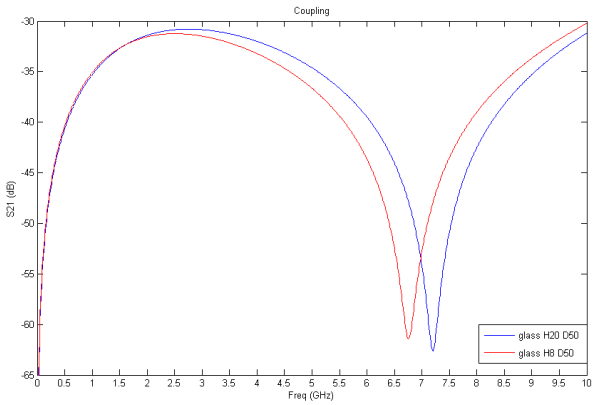


Fig. 8. Simulated response of two 50μm apart inductors in glass substrate

According to the current density and magnetic field distribution (Figure. 10 and 11), we can clearly see what happens when two inductors coupled. For better expression, the left one is called the main inductor and the right one is called the secondary one. In case of only the main one is added excitation, the existence of the secondary inductor makes the current density of the main one's outer coil stronger. At the same time, in the secondary one the electric field of the area closed to the main inductor becomes stronger too. In case of two inductors are both added excitations, the coupling between them can be recognized by weakening of current density because they have the same current direction. Fig. 11 shows the change of magnetic field when the inductors couple.

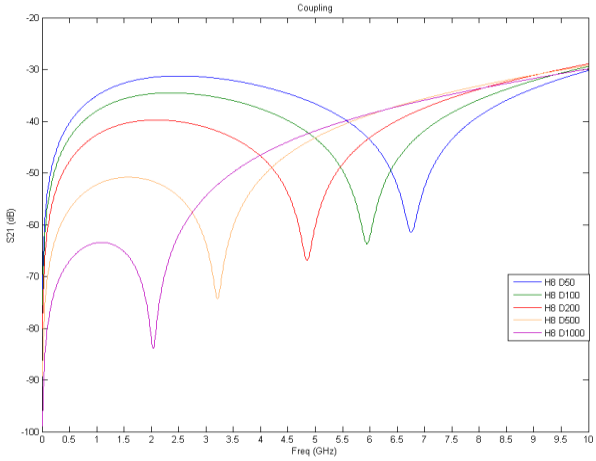
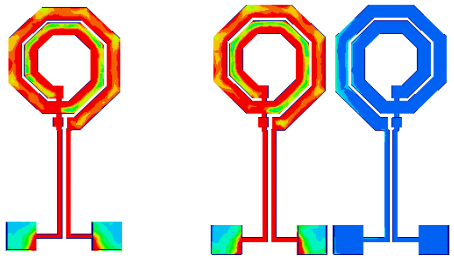
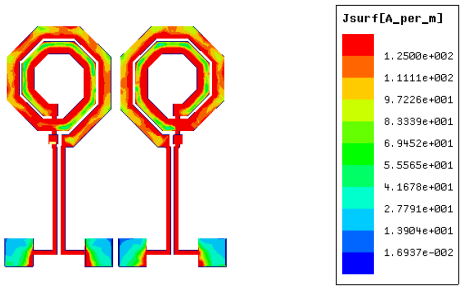


Fig. 9. Simulated response of two inductors in glass substrate

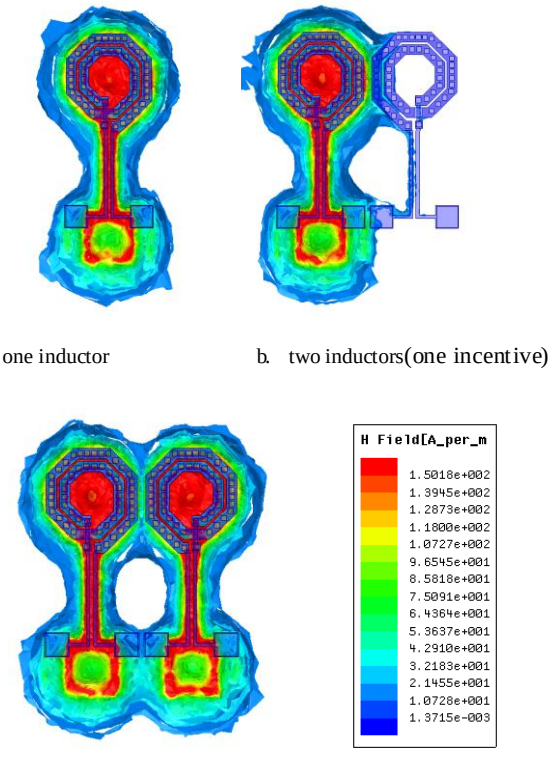


a. one inductor b. two inductors(one incentive)



c. two inductors (two incentive)

Fig. 10. Current density distribution of inductors



a. one inductor b. two inductors(one incentive)

c. two inductors (two incentive)

Fig. 11. Magnetic field distribution of inductors

V. CONCLUSION

In this paper, we design inductors on silicon and glass substrates and some electric analysis was performed to study the effects of the metal layers and substrate and the coupling of two inductors. The key achievements in this work are summarized as follow:

1) Electrical performances of inductors with one and two metal layers have been studied. Thick metal layers can reduce the inductance L. And this applies in both single-layer and double-layer inductors and both on silicon and glass substrates.

2) The comparison of electrical properties between thin-film IPD on silicon substrate and glass substrate is given. The Q-factor of the inductor on glass substrate is larger than its corresponding structure on silicon substrate at high frequencies.

3) Two models of the same two inductors placed side by side were used to study the coupling between them. Glass substrates reduce the coupling in high-frequency, although it makes the resonance point move towards high-frequency. The increasing of the thickness of the metal layer affects the coupling in the same way as glass substrate does. Increasing the distance of two inductors reduces the coupling in low-frequency, as well as makes the resonance point move towards the low-frequency greatly.

ACKNOWLEDGMENT

This work was financially supported by the National S & T Major Project under contract No. 2013ZX02501.

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