Influence of thermal annealing on the deformation of Cu-filled TSV

Hongwen He[a,b], Xiangmeng Jing[a,b], Liqiang Cao[a,b], Daquan Yu[a,b], Kai Xue[a], Wenqi Zhang[a]
[a]National Center for Advanced Packaging (NCAP China)
[b]Institute of Microelectronics of Chinese Academy of Sciences
[a] Building D1, Sensor Network International Science Park, Wuxi, Jiangsu, PR China
[b] No. 3, Bei-Tu-Cheng West Road, Beijing, PR China
Corresponding author e-mail: hongwenhe@ncap-cn.com or caoliqiang@ime.ac.cn;

Abstract

Through silicon via (TSV) is regarded as one of the most advanced packaging technologies, however, many serious reliability issues need to be paid more concerns. The Cu pumping effect is one of the most crucial reliability problems. Due to different coefficient of thermal expansion for different packaging materials, Cu-TSV can deform and damage the wiring redistribution layers and degrade the reliability of the package as a whole during normal processing. Therefore, this work focuses on the influence which different thermal annealing processes have on Cu pumping in Cu-filled TSVs. Cu TSVs having 20μm in diameter and 120μm in depth were fabricated on 200 mm wafers by etching, insulation layer deposition, barrier layer deposition, seed layer deposition and Cu plating in sequence. Then the wafer surface was polished to remove the excessive Cu. Two anneal approaches were designed to investigate Cu TSV pumping. One was CMP first before annealing, and the other was annealing before CMP and followed by the 2nd annealing. Anneal tests were done in a nitrogen environment to protect Cu from oxidation. The annealing temperatures were set at 300°C and 400°C with a dwell time of 40min. The degree of pumping was evaluated by measuring the height and volume profiles before and after annealing by using a white light interferometer. Results show that the Cu TSV increased by 0.105μm and 0.168μm in height and 90.443μm^3 and 93.993μm^3 in volume at 300°C and 400°C with CMP first approach. However, the Cu TSV increased by only 0.066μm and 0.075μm and 30.797μm^3 and 10.077μm^3 in volume at 300°C and 400°C with anneal first approach. It can be concluded that the Cu pumping effect may be restrained by anneal first approach.

Introduction

With electronic devices become smarter and multifunctional, particularly portable devices such as mobile phones and notebooks, more chips need to be stacked together without increasing the package size [1, 2]. 3D packages are increasingly being adopted to realize vertical interconnect for stacking more chips, which helps in significantly reducing wiring lengths, interconnection latency, and power dissipation while enhancing performance. Through silicon via (TSV) is a key enabling technology for 3D IC integration which assists in the realization of high miniaturized and complex next-generation systems [3]. Current efforts are mostly focused on the development and improvement of TSV fabrication process, efforts to study in-depth the associated reliability issues in TSVs are still limited [4, 5]. Thermo-mechanical reliability is one of the main reliability concerns, because process conditions during subsequent bumping and die-stacking processes subject the wafers to repeated thermal loadings. Due to the mismatch in coefficient of thermal expansion (CTE) between copper, surrounding dielectric, and silicon substrate, thermal stresses can be developed in the silicon and interconnect structures, resulting in several reliability problems such as cracking, delamination, and voiding [6]. During TSV annealing and subsequent fabrication processes, Cu TSVs were found to extrude out of the Si wafer surface, causing fracture of the overlying dielectric material. This is a potential threat to the IC interconnection layer, particularly for low-k materials, since it can lead to cracking of the dielectric layer in the BEOL structure. It was observed that, if the TSVs have not received proper heat treatment prior to backside processing, it will bulge upwards and deform the metal/dielectric stack on top. Previous studies have reported that initial heat treatment at 420°C for 20 min could solve the TSV protrusion [7]. It is analyzed that, during the first thermal cycling, the Cu via undergoes material transformation, such as grain growth and recrystallization, thus resulting in an open hysteresis loop. The succeeding cycles after the first cycle are found to have the loops that are similar in shape, size, and position. This means that the material behavior of Cu becomes stable after the first cycle to the maximum thermal cycling condition [8, 9]. Therefore, suitable heat treatment and non-destructive detecting the TSV deformation and stress are of great importance for TSV based 3D integration.

Therefore, in this work, annealing process with different temperatures of 300°C and 400°C with dwell time of 40min on the Cu-filled TSV interposer was investigated with N_2 protection from oxidation. Two anneal approaches were designed, one was CMP first before annealing, and the other was annealing before CMP and followed by the 2nd annealing. The Cu protrusion quantity was characterized by the white light interferometer (WLI).

Experimental

The 200mm wafer was selected for the TSV interposer fabrication, where the aspect ratio of the TSV was about 6:1, 20μm in diameter and 120μm in depth. The pitch of the Cu-TSVs was 100μm. The tested silicon wafer was etched by deep reactive ion etching (DRIE) method. Subsequently, the silicon oxide as the insulation layer with 2μm thickness was deposited by chemical vapor deposition with TEOS. A titanium barrier layer with 200nm thickness, followed by a seed layer of copper with 1μm thickness, was deposited by physical vapor

deposition method. The wafer was electroplated with Cu by bottom-up mode. Finally, the whole wafer was diced into 4mm×4mm samples for anneal test. Two samples were grinded and polished to remove the surface Cu and insulation layer to reveal the Cu vias, and another two samples were conducted after anneal test. The dimension of the samples was shown in Fig.1.

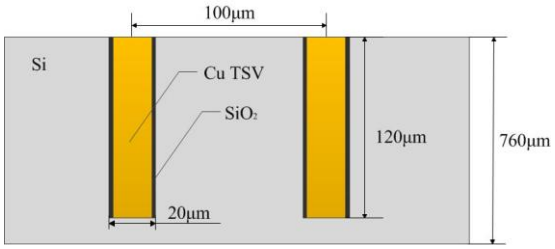


Fig.1 Schematic drawing of the TSV interposer

Before anneal experiment, the tested samples were rinsed by ethanol and deionized water to remove the residual impurity. Marks were designed and branded at the interested region, which can conveniently realize the in-situ observation of the same Cu via. Thermal anneal tests were conducted in a N_2 environment to protect Cu vias from oxidation. The annealing temperatures were set at 300°C and 400°C with dwell time of 40min, respectively. In order to understand the anneal process effect on the Cu vias, the Cu via morphology was detected by the white light interferometer to confirm the original Cu height and volume before and after the anneal test.

Results and discussion

Fig.2 illustrates an optical picture of the polished TSV array. Fig.3 shows the cross section of bottom up filled vias and the 3D X-ray image. All the vias are void free filled successfully. The overburden is removed by chemical mechanical polishing (CMP). With the slurry provided by Anji Microelectronic Inc., the TSV wafer is polished at 5 PSI down force and 50 rpm rotation speed for 30 minutes.

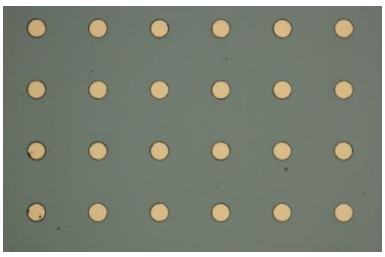


Fig. 2 Optical morphology of the polished TSV array

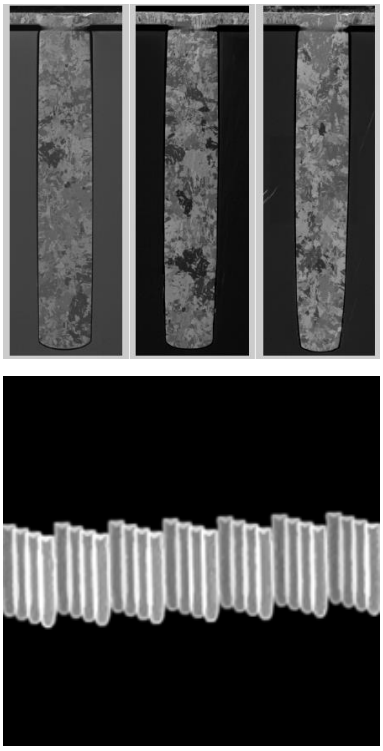
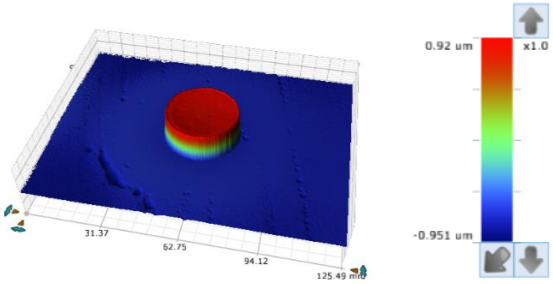
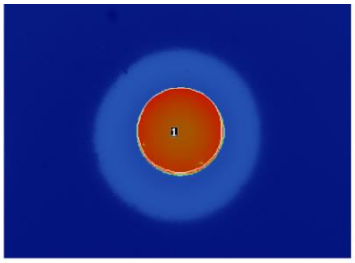


Fig. 3 Images of the cross section of the filled vias and their 3D X-ray image

The white light interferometer (WLI) technique is a convenient, high resolution, noncontact method, which can meet the need of small measurement range and high resolution simultaneously. As De Wolf has pointed out and testified that using white light interferometer is the faster and reliable way to measure the Cu via height than that of the atomic force microscopy and contact probe method [10]. Therefore, it is rightly used in this study to characterize the Cu via protrusions. Fig.4 shows the typical morphology of the Cu via by the WLI before anneal test. It can be clear seen from fig.4 (a) that the Cu vias have been protruded out of the surface after CMP process in the vertical direction. In other words, the CMP process has polished away the Cu layer and silicon oxide layer on the top surface. Importantly, the top surface is rather smooth and the top center part of the Cu via is polished more than that at the marginal region, which appears dishing effect. Fig. 4(b) shows the height and volume results measured by the analyzing software of the WLI.



(a) Cu-TSV morphology measured by WLI

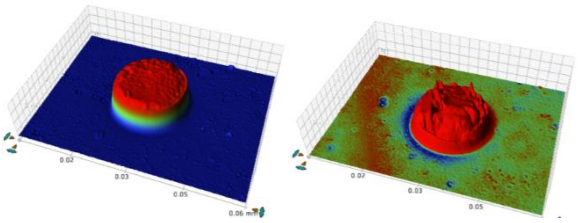


No	Region	Rp µm	Rp% µm	Volume µm³
1		0.968	0.939	634.617

(b) Height and volume results measured by the analyzing software of the WLI

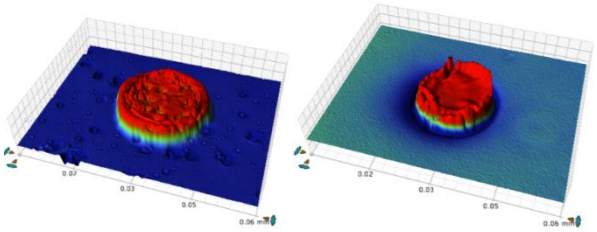
Fig.4 Morphology of the Cu via before anneal test

Fig.5 shows the morphology evolution of the Cu vias by the WLI after anneal test with CMP first, where Fig.5 (a) is annealed at 300°C, and Fig. 5(b) is annealed at 400°C. Fig.6 shows the morphology evolution of the Cu vias with anneal first, then with CMP process and followed by the second anneal test. Fig.6 (a) is annealed at 300°C, and Fig. 6(b) is annealed at 400°C. From the images we can find that the Cu vias are protruded again in the vertical direction. This can be further testified by the measured data in Tab. 1, which lists the height and volume evolution of the Cu vias with different temperatures and anneal conditions. Moreover, as the temperature increases, the top surfaces of the Cu vias become not smooth any more.



(a) 300°C (b) 400°C

Fig. 5 Cu-TSV morphology after anneal test with CMP first approach



(a) 300°C (b) 400°C

Fig. 6 Cu-TSV morphology after anneal test with anneal first approach

As the anneal temperatures were 300°C and 400°C with CMP first, the height of the Cu via increased by 0.105µm and 0.168µm, respectively. Accordingly, the volumes increased by 90.443µm and 93.993µm, respectively. It meant that the height and volume of the Cu vias increased as the anneal temperature increased from300°C to 400°C. However, as the anneal test conducted twice, the height and volume evolution increased not so much as that with CMP first condition. The height of the Cu via increased by 0.066µm and 0.075µm and the volume increased by 30.797µm and 10.077µm, respectively. In total, both the anneal tests can make the Cu pumping through the vertical direction, however, anneal first condition can effectively restrain the Cu pumping as compared with CMP first condition.

Tab. 1 Height and volume evolution of the Cu vias

No	Tpye	T/°C	t/min	H/µm	V/µm
1	CMP first	300	40	0.105	90.443
2	CMP first	400	40	0.168	93.993
3	Anneal first	300	40	0.066	30.797
4	Anneal first	400	40	0.075	10.077

As the anneal temperature rapidly increases to the target setting, all the component in the Cu TSV including Cu, silicon oxide, Ti and silicon expand. However, due to the comparative high CTE of the Cu relative to Si, a compressive stress is built up in the Cu via. As the temperature and dwell time are high enough, the stress must be relaxed by some modes, such as creep or diffusion. Because the Cu is restrained by the surrounding Si, the only possible diffusion path is on the top surface. Thus, the relaxation results in an extrusion of the copper. As the Cu TSV cools down quickly, there is no complete retraction of the copper, leaving a slight protrusion above the Si surface [1, 2]. According to anneal first approach, the Cu vias are surrounded by insulation layer and top surface layers. Therefore, the deformation of the Cu vias was suppressed. As the sample was polished and underwent the second anneal process, less stress was triggered as compared to the CMP first approach, leading to less Cu pumping.

Conclusions

This work investigated the effect of different annealing process with different temperatures of 300°C and 400°C and dwell time of 40min on the Cu-filled TSV interposer. The evaluation of the pumping degree was obtained by analysis of height and volume profiles before and after anneal test by the white light interferometer. Results show that the Cu TSV increased by 0.105µm and 0.168µm in height and 90.443µm^3 and 93.993µm^3 in volume at 300°C and 400°C with anneal approach once. However, the Cu TSV increased by only 0.066µm and 0.075µm and 30.797µm^3 and 10.077µm^3 in volume at 300°C and 400°C with anneal approach twice. It concluded that anneal first condition and then CMP followed by the second anneal condition can reduce the Cu pumping effect.

Acknowledgments

The authors acknowledge the support of National Science and Technology Major Project (Project number：2013ZX02501)

References

[1] P. Kumar, I. Dutta, “Influence of electric current on diffusionally accommodated sliding at hetero-interfaces,” Acta Materialia, 2011, vol. 59, pp. 2096-2018.

[2] I. Dutta, P. Kumar, and M.S. Bakir, “Interface-related reliability challenges in 3-d Interconnect Systems with through-Silicon Vias,” JOM, 2011, vol. 63, pp. 70-77.

[3] Suk-Kyu Ryu, Qiu Zhao, Michael Hecker, et al., “Micro-Raman spectroscopy and analysis of near-surface stresses in silicon around through-silicon vias for three-dimensional interconnects,” J. Appl. Phys., 2012, 063513

[4] W. S. Kwon, D. T. Alastair, K. H. Teo, et al. “Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy,” Appl. Phys. Lett., 2011, 232106

[5] Holger Roth, Zhenhui He, Thomas Mayer, “Inspection of Through Silicon Vias (TSV) and other Interconnections in IC packages by Computed Tomography,” 11th Electronics Packaging Technology Conference, Singapore 2009

[6] Sven Niese, Peter Krueger, Ehrenfrid Zscheh, “NanoXCT-A High-Resolution Technique for TSV characterization,” AIP Conf. Proc. 2011, pp. 168-173

[7] Holger Roth, Tobias Neubrand, “Non-destructive Inspection of through Mould vias in Stacked Embedded Packages by Micro-CT,” 13th Electronics Packaging Technology Conference, Singapore 2011, pp. 710-713

[8] L. W. Kong, J. R. Lloyd, K. B Yeap, et al, “Applying x-ray microscopy and finite element modeling to identify the mechanism of stress-assisted void growth in through-silicon vias,” JOURNAL OF APPLIED PHYSICS, 2011, pp. 053502

[9] Holger Roth, Tobias Neubrand, Thomas Mayer, “Improved Inspection of Miniaturised Interconnections by Digital X-ray Inspection and Computed Tomography,” 12th Electronics Packaging Technology Conference, Singapore 2010, pp.441-444

[10] De Wolf, K. Croes, O. Varela Pedreira, R. Labie, A. Redolfi, M. Van De Peer, et al., “Cu pumping in TSVs: Effect of pre-CMP thermal budget,” Microelectronics Reliability, 2011, vol. 51, pp. 1856-1859